User's Guide

Agilent Technologies
N5102A Baseband Studio Digital Signal Interface Module

Due to our continuing efforts to improve our products through firmware and hardware revisions, N5102A module design and operation may vary from descriptions in this guide. We recommend that you use the latest revision of this guide to ensure you have up-to-date product information. Compare the print date of this guide (see bottom of page) with the latest revision, which can be downloaded from the following website:

www.agilent.com/find/basebandstudio

Agilent Technologies

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1 Installation

This chapter provides the following:

Safety Information

Warnings, Cautions, and Notes

The following safety notations are used throughout this manual. Familiarize yourself with each notation and its meaning before operating this product.

WARNING	*Warning* denotes a hazard. It calls attention to a condition or situation that could result in personal injury or loss of life. Do not proceed beyond a warning until the indicated conditions or situations are fully understood.

CAUTION	*Caution* calls attention to a possible condition or situation that could result in a loss of a user's work, damage, or destruction of the product. Do not proceed beyond a caution until the indicated conditions are fully understood.

NOTE	*Note* calls the user's attention to an important point of special information within the text. It provides operational information or additional instructions of which the user should be aware.

Instrument Markings

The following markings are is used on the N5102A Baseband Studio digital signal interface module. Familiarize yourself with it and its meaning before operating the module.

CE The CE mark is a registered trademark of the European Community. If this symbol is accompanied by a year, it is the year when the design was proven.

CSA The CSA mark is a registered trademark of the Canadian Standards Association.

N10149 The C-Tick Mark is a trademark registered to the Australian Spectrum Management Agency. This indicates compliance with all Australian EMC regulatory information.

This symbol indicates that the center conductor (of the power supply) is positive, and the outer conductor is negative.
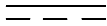
This symbol indicates that the input power required is DC.
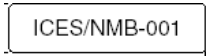
ICES/NMB-001 This symbol indicates compliance with the Canadian Interference-Causing Equipment Standard (ICES-001).

General Safety Considerations

WARNING **Personal injury may result if the module cover is removed. There are no operator serviceable parts inside. To avoid electrical shock, refer servicing to qualified personnel.**

Getting Started

Checking the Shipment

1. Inspect the shipping container for damage.

   Signs of damage may include a dented or torn shipping container or cushioning material that indicates signs of unusual stress or compacting.

2. Carefully remove the contents from the shipping container and verify that your order is complete.

   The following items are shipped standard with each N5102A Baseband Studio digital signal interface module:

   • user's guide

   • documentation CD-ROM

   • three-prong AC power cord (specific to geographic location)

   • power supply

   • proprietary three-meter digital bus cable

   • five break-out boards (PC boards with connectors)

   • loop back fixture (for troubleshooting)

   • Device Interface port mating connector
     See for connector locations.

Instrument Dimensions

Length: 189.9 mm (7.48 in)

Width: 144.8 mm (5.70 in)

Height: 41.6 mm (1.64 in)

Meeting Electrical and Environmental Requirements

The N5102A module is designed for use in the following environmental conditions:

• indoor use
• altitudes < 15,000 feet (4,572 meters)
• 0 to 55°C temperatures, unless otherwise specified

- 80% relative humidity (maximum for temperatures up to 31°C, decreasing linearly to 50% relative humidity at 40°C.

CAUTION   This product is designed for use in INSTALLATION CATEGORY II and POLLUTION DEGREE 2, per IEC 61010-1 and 664, respectively.

Ventilation

Ventilation holes are located on the front and rear panels of the N5102A module. Do not allow these holes to be obstructed, as they allow air flow through the module.

When installing the module in a cabinet, the convection into and out of the module must not be restricted. The ambient temperature outside the cabinet must be less than the maximum operating temperature of the module by 4°C for every 100 watts dissipated within the cabinet.

CAUTION   Damage to the module may result when the total power dissipated in the cabinet is greater than 800 watts. When this condition exists, forced convection must be applied.

Line Settings

The *N5102A module* requires a power supply that meets the following conditions:

Voltage: 5V

Frequency: DC

Current: 4.0A

The module's *power supply* requires a power source that meets the following conditions:

Voltage: 100–240V

Frequency: 50–60 Hz

Current: 0.7A

CAUTION   Damage may result if a supply voltage is not within its specified range.

Connecting the AC Power Cord

This is a Safety Class 1 Product provided with a protective earth ground incorporated into the power cord. The AC power cord is the device that disconnects the mains circuits from the mains supply. In addition, an external circuit breaker, readily identifiable and easily reached by the operator, should be available for use as the disconnecting device. Use the following steps to connect the AC power cord:

WARNING	**Personal injury may occur if there is any interruption of the protective conductor inside or outside of the product. Intentional interruption is prohibited.**

CAUTION	Damage to the product may result without adequate earth grounding. Always use the supplied three-prong AC power cord.

1. Ensure that the power cord is not damaged.

2. Install the product so that one of the following items is readily identifiable and easily reached by the operator: AC power cord, alternative switch, or circuit breaker.

3. Insert the mains plug into a socket outlet provided with a protective earth grounding.

AC Power Cord Localization

The AC power cord included with the module is appropriate for the final shipping destination. You can, however, order additional AC power cords for use in different areas: see "Replaceable Parts" on page 100.

Proper Usage and Cleaning

The N5102A module cover protects against physical contact with internal assemblies that contain hazardous voltages, but does not protect against the entrance of water. To avoid damage and personal injury, ensure that liquid substances are positioned away from your N5102A module.

WARNING	**Personal injury may result if the N5102A module is not used as specified. Unspecified use impairs the protection provided by the equipment. The N5102A module must be used with all means for protection intact.**

Cleaning Suggestions

To prevent dust build-up that could potentially obstruct ventilation, clean the N5102A module cover periodically. Use a dry cloth, or one slightly dampened with water, to clean the external case parts.

WARNING   **Electrical shock may result if the N5102A module is not disconnected from the mains supply before cleaning. Do not attempt to clean internally.**

Connecting the N5102A Module to the ESG/PSG

The N5102A module is used with an Agilent E4438C ESG[1] or E8267C PSG[2] signal generator; the signal generator provides baseband data to the interface module. This section provides information on connecting the N5102A module to the signal generator. While the graphics show an ESG signal generator, the procedure is the same for the PSG.

CAUTION	The digital bus cable connector has a release latch on each side (as shown below). To avoid connector damage, simultaneously squeeze both release latches when connecting or disconnecting the cable. A securely connected cable does not come loose when gently pulled.

Digital bus cable connector release latches

Press the release latches when connecting or disconnecting the cable.
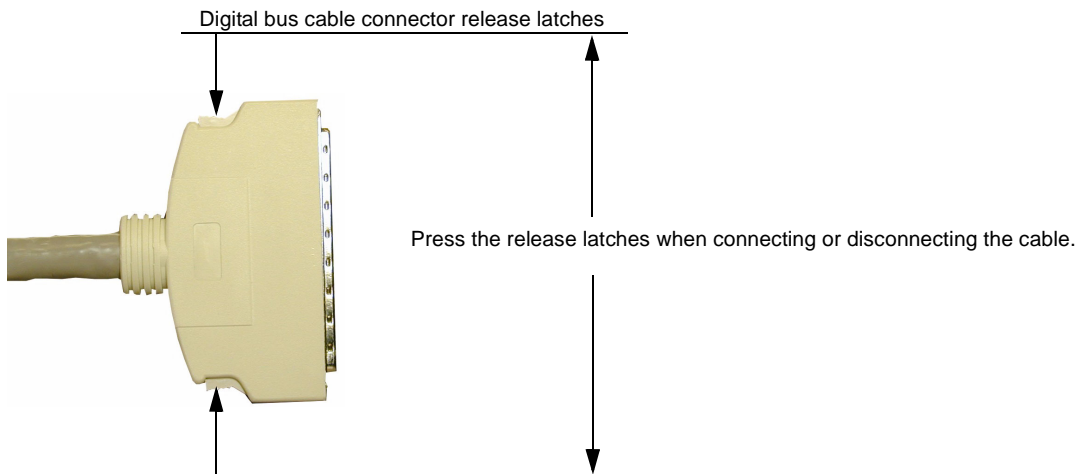
1. Refer to Figure 1-1. Connect the end of the digital bus cable that has the EMI suppressor to the signal generator's rear panel digital bus connector.

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[1]Requires Options 003 and either 601 or 602.
[2]Requires Options 003 and 602.

NOTE	The digital bus connector may be labeled as DIGITAL BUS, DIG I/Q I/O, or DIGITAL I-Q I/O.

Figure 1-1   **Signal Generator Digital Bus Cable Connection**

Press the release latches when connecting or disconnecting the cable.

EMI Suppressor
Attach this end of the cable to the signal generator.

Press the release latches when connecting or disconnecting the cable.
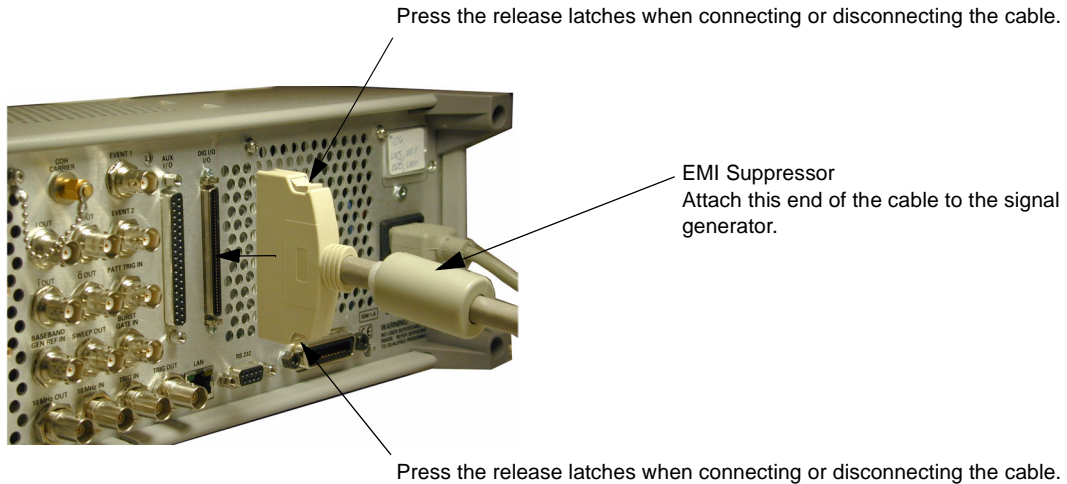
2. Refer to Figure 1-2. Connect the other end of the digital bus cable to the Digital Bus connector on the N5102A module.

The proprietary three meter cable enables you to place the interface module in a location close to the device under test (DUT).

Figure 1-2   **N5102A Module Digital Bus Cable Connection**

Press the release latches when connecting or disconnecting the cable.
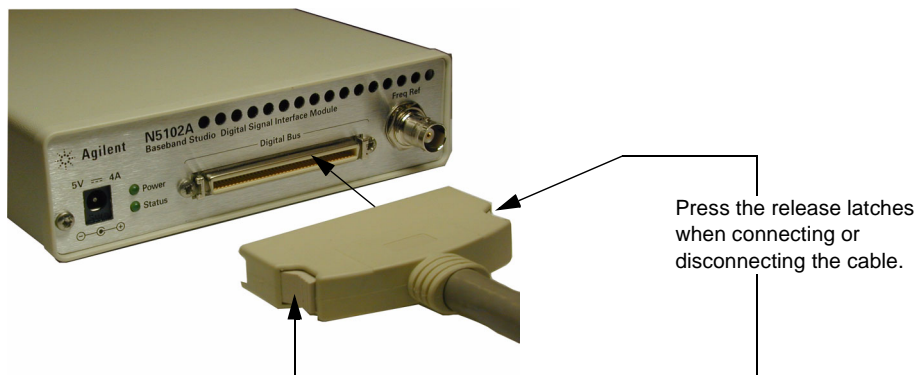
3. Refer to Figure 1-3. Connect the AC power cord to both the power supply and the AC power source (for details on connecting an AC power cord to an AC power source, see "Connecting the AC Power Cord" on page 6).

4. Connect the power supply to the N5102A module DC power receptacle.

Figure 1-3   **N5102A Module Power Supply Connections**

AC Power Connection   **DC Power Connection**
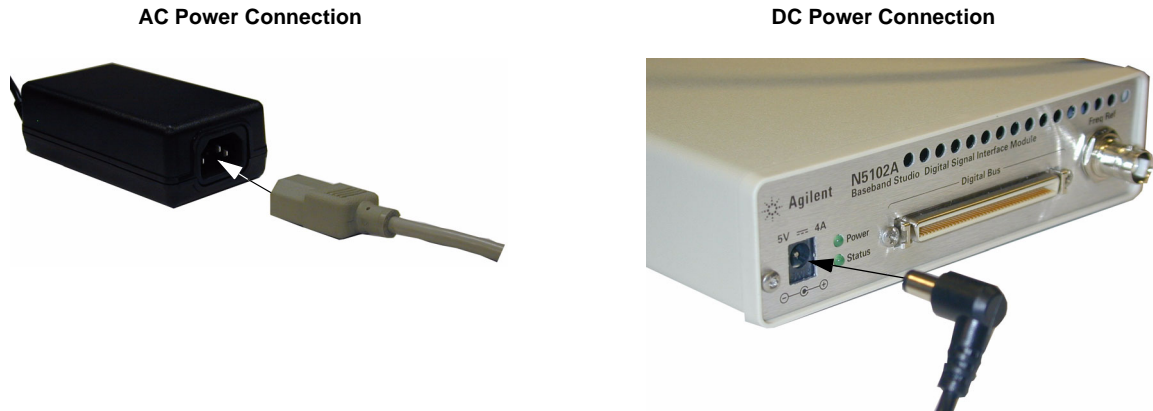
The power LED should be illuminated, indicating that the interface module is connected to the power source. If the power LED is not illuminated, check the AC power connection for the power supply and ensure that the DC power supply plug is fully inserted into the N5102A module DC power receptacle. If problems still persist after checking the power cords, refer to Chapter 6, "Troubleshooting," on page 93.

Figure 1-4 shows a completed installation.

Figure 1-4   **Completed N5102A Module Installation**

Power LED is illuminated
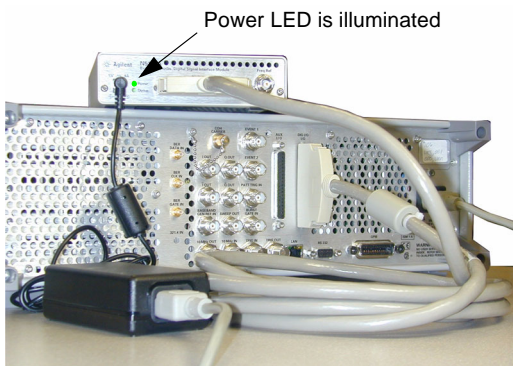
Operation Verification

The N5102A module is configured and controlled using the user interface (UI) on the ESG/PSG signal generator. The operation verification uses the device interface test (Device Intfc), which is one of four interface module diagnostic tests, referred to as loop back tests. This loop back test checks the complete setup, providing a high level of confidence that the system is functioning properly. The three other tests are used if this test fails, and are described in "Running Diagnostic Tests" on page 96.

CAUTION	The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

1. Connect the N5102A module to the signal generator (as described in "Connecting the N5102A Module to the ESG/PSG" on page 8).

2. Refer to Figure 1-5. Connect the Loop Back Test Single Ended IO Dual 40 Pin board to the Device Interface connector on the rear panel of the N5102A module.

Figure 1-5   Connecting the Loop Back Board to the N5102A Module
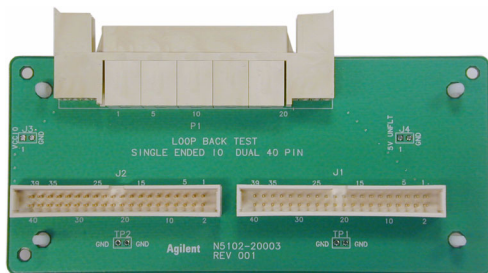
Loop Back Test Single Ended IO Dual 40 Pin Board   Connecting the Board to the Device Interface Connector
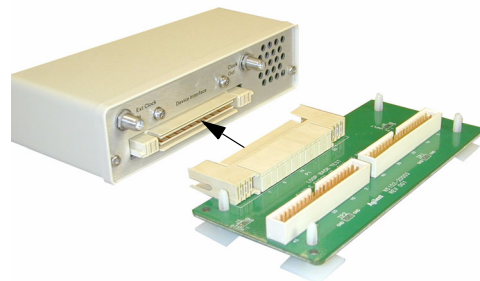
The Loop Back Test Single Ended IO Dual 40 Pin board is used both for loop back testing, and as a break-out board to simplify the connection between the N5102A module and the DUT. When used for loopback testing, there should be no connections to the dual 40-pin connectors.

3. If the signal generator is not already on, turn it on.

4. On the signal generator, select the device interface test:

Press **Aux Fctn** > **N5102A Interface** > **Diagnostics** > **Loop Back Test Type** > **Device Intfc**.

As shown in Figure 1-6, the currently selected test is displayed in parenthesis below the
Loop Back Test Type softkey. Note also that the graphic provided displays the current test setup.

Figure 1-6   ESG/PSG Diagnostic Test Display

Selected loop back test

Loop back test setup
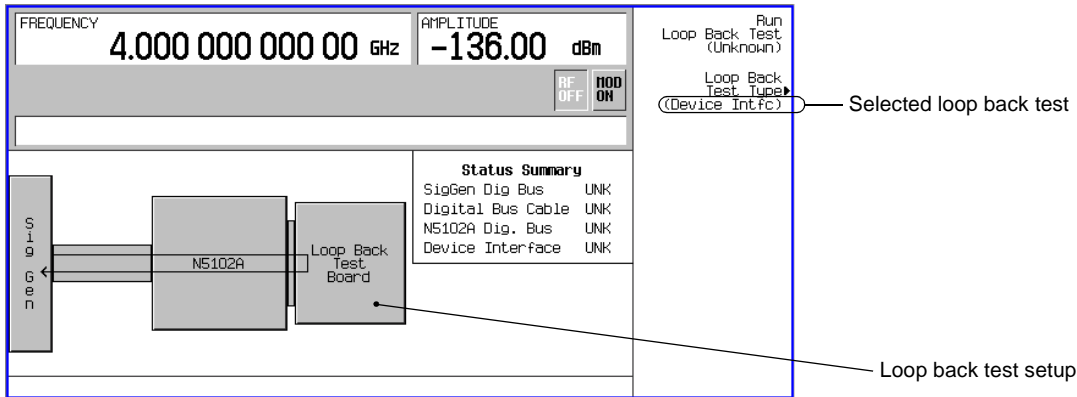
5. Run the selected test: press **Run Loop Back Test**.

When the test completes, the results of the test (pass or fail) replaces unknown in both the
parenthesis with the softkey and in the Status Summary display as shown in Figure 1-7. If
this test fails, refer to "Running Diagnostic Tests" on page 96.

Figure 1-7   ESG/PSG Loop Back Test Result

Loop back test results
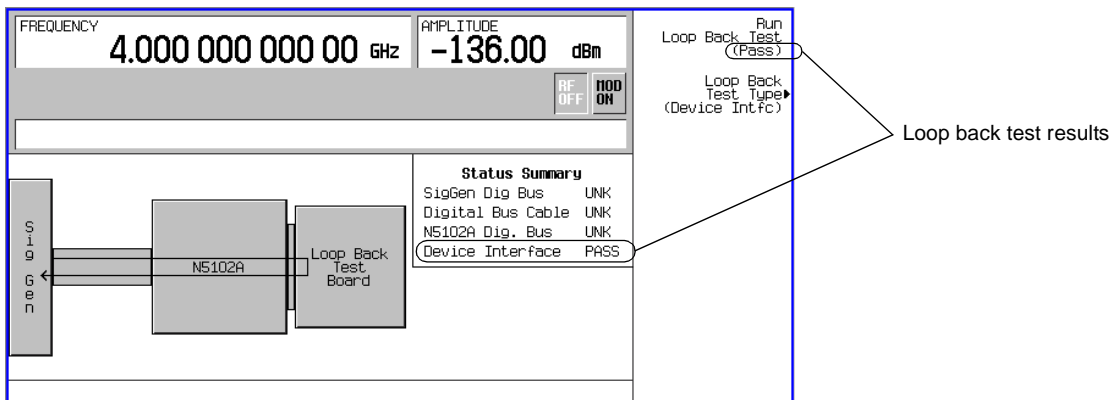
Regulatory Information

Statement of Compliance

This product has been designed and tested in accordance with IEC Publication 61010, *Safety Requirements for Electronic Measuring Apparatus*, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Agilent Technologies products. For any assistance, contact Agilent Technologies (see).

Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory.

• this product does not require calibration

Declaration of Conformity

A declaration of conformity is on file for this product, and a copy is available upon request.

Compliance with German Noise Requirements

This is to declare that this instrument is in conformance with the German Regulation on Noise Declaration for Machines (Laermangabe nach der Maschinenlaermrerordnung –3.GSGV Deutschland).

Table 1-1   German Noise Requirements

Acoustic Noise Emission/Geraeuschemission	
LpA < 70 dB	LpA < 70 dB
Operator position	am Arbeitsplatz
Normal position	normaler Betrieb
per ISO 7779	nach DIN 45635 t.19

Compliance with Canadian EMC Requirements

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB du Canada.

2 Overview

This chapter describes the features of the N5102A Baseband Studio digital signal interface module along with the signal generator options required to operate it.

Features

The N5102A Baseband Studio digital signal interface module works with the Agilent E4438C ESG[1] or E8267C PSG[2] vector signal generators to provide a flexible digital interface for delivering digital baseband (IQ) or digital intermediate frequency (IF) test signals. The complex modulation formats of the signal generators, including W-CDMA, multitone, 1xEV-DV, WLAN and many more, are available at the bit level for testing digital components, transceivers, and subsystems. The N5102A module delivers the digital IQ or digital IF signals to your device with the data requirements, clock features, and signaling you need. With its selection of logic types and break-out board connectors, the interface module connects easily into your test system, in most cases eliminating the need for custom fixtures.

The N5102A module provides many features:

- bit level access to arbitrary waveform generator (ARB) and real-time signal generator baseband data from a wide range of signal creation applications

- simple user interface

- flexible data formats

  — variable 4- to 16-bit word size

  — serial, parallel, and parallel interleaved data transmission

  — 2's complement or offset binary word representation

  — MSB or LSB bit order

  — digital IQ or digital IF signal

- flexible clocking

  — automatic resampling

  — 1 kHz to 100 MHz sample rate

  — multiple clock inputs and outputs

  — adjustable clock phase and skew

  — multiple clocks per sample up to 4x

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[1]Requires Options 003 and either 601 or 602.
[2]Requires Options 003 and 602.

- flexible signal interface

  — multiple logic types provide single ended and differential testing capability—low voltage TTL (LVTTL), LVDS, and CMOS 1.5 V, 1.8 V, 2.5 V, and 3.3 V

  — proprietary three meter cable connects the N5102A module to the signal generator

  — interchangeable break-out boards

The parameters for the N5102A module are set using the UI on the ESG/PSG signal generators. This provides you with familiar UIs for both the modulation format and the interface module. Option 003 on the ESG/PSG enables the N5102A module UI.

With the N5102A module connected to the signal generator, you can perform multiple levels of testing. Since the baseband data that is provided to the interface module is the same data that can be modulated onto the RF carrier, this provides the benefit of performing early-stage testing of digital components and subsystems with the N5102A module, and then testing the integrated system using the modulated RF carrier.

Front Panel

The baseband data and frequency reference inputs for the N5102A module are located on the front panel along with the receptacle for the DC power. A Power LED on the front panel indicates when DC power has been applied and a Status LED shows when the data lines are active.

Figure 2-1   **Front Panel Features**
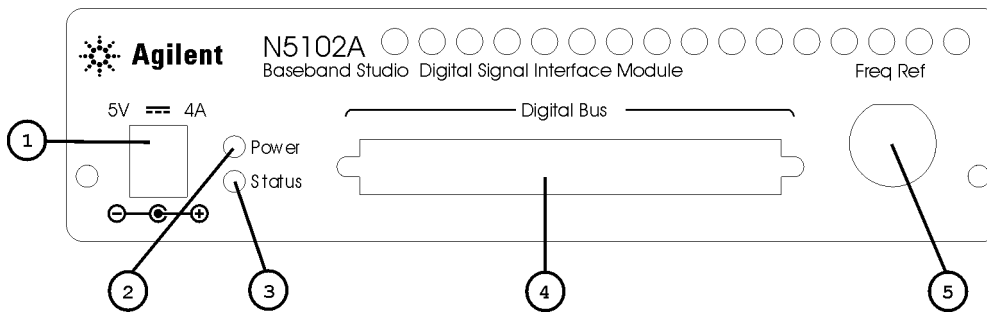
1. DC Power Receptacle

This receptacle accepts the DC power cord from the power supply. The DC power cord is shipped with the interface module.

2. Power LED

This LED illuminates when DC power is supplied to the N5102A module.

3. Status LED

The LED illuminates when the interface module is first turned on by pressing the **N5102A Off On** softkey located in the signal generator UI or after performing a module diagnostic test. Once lit, the LED stays on until the DC power is removed from the interface module. The LED conveys the status of the data lines and has two modes of operation:

Blinks Rapidly   This indicates that the data lines are active and ready to transmit or are transmitting a digital signal.

Solid Illumination   This shows that the data lines are inactive.

4. Digital Bus Connector

This is the connector that the N5102A module uses to communicate with the ESG/PSG signal generator. A proprietary three-meter digital bus cable is supplied that connects to the Digital Bus connector and facilitates placing the interface module in a location close to the DUT.

5. Freq Ref Connector

When Internal is the selected clock source, this 50 ohm connector accepts an external frequency reference at 3 dBm ±6 dB within the frequency range of 1 to 100 MHz that is used to generate the internal clock signal.

CAUTION	It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

Rear Panel

The rear panel contains three connectors that are shown in Figure 2-2 and described in the following sections.

Figure 2-2   **Rear Panel Features**
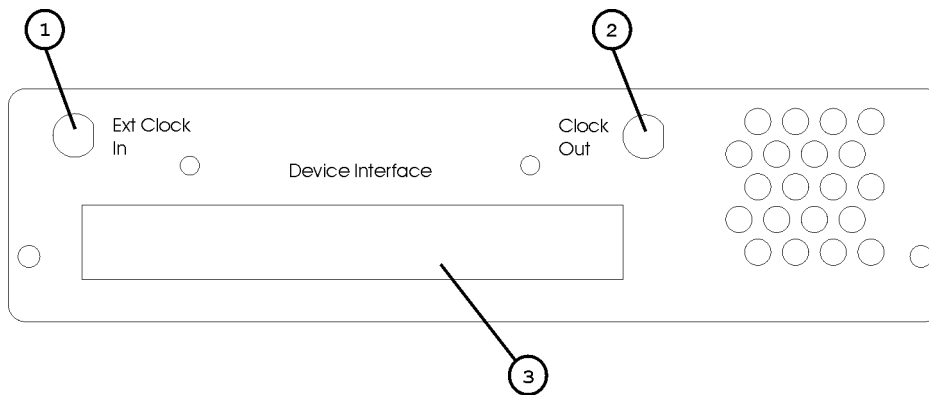
1. Ext Clock In Connector

This AC coupled 50 ohm connector is used for connecting an external clock source to the N5102A module. It accepts a signal with a nominal amplitude of 0 dBm and has a frequency range of 1 MHz to 400 MHz.

CAUTION	It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

2. Clock Out Connector

This 50 ohm connector outputs the clock signal at a nominal 400 mVp-p level with a frequency range of 100 kHz to 400 MHz. For a high impedance load of 5 kΩ or higher, the frequency range changes to 1 kHz to 100 kHz with a nominal output level of 2 Vp-p.

3. Device Interface Connector

This connector interfaces with the DUT and supplies the digital IQ and digital IF signals in addition to sense lines, ground connections, a DC supply, and input and output clock signals. For more information on this connector including its pin-out, see "Device Interface Connector" on page 34.

CAUTION   The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

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3 DUT Connections

This chapter provides information for the N5102A Baseband Studio digital signal interface module Device Interface connector, the supplied break-out boards, and the device interface mating connector to help simplify the DUT connection.

- "Break-Out Boards" on page 24
- "Device Interface Connector" on page 34
- "Device Interface Mating Connector" on page 39

Break-Out Boards

This section describes the different break-out boards and provides the pin-out for each one.

To maximize signal integrity, make the DUT connection as close as possible to the N5102A module Device Interface connector. The supplied break-out boards aid in minimizing this distance. Another solution is to incorporate the supplied device interface mating connector onto the DUT, eliminating the need for the break-out board and connecting cables.

Five interchangeable break-out boards are supplied to simplify the connection between the DUT and the N5102A module. The break-out boards connect to the Device Interface connector on the rear panel of the module and each comes with a different type of output connector. This provides a wide range of connection possibilities for the DUT. The break-out boards are easily identified by their output connector. If the situation arises where none of the break-out boards meet your needs, you can customize a connection solution using the supplied device interface mating connector. See "Device Interface Connector" on page 34 and "Device Interface Mating Connector" on page 39 for information. Table 3-1 lists the five break-out boards and the test type for which each is intended.

Table 3-1   Break-Out Board List

Break-Out Board	Test Type	Comment
Single Ended I/O Dual 20 Pin	Single-ended	0.1 inch spaced header This connector is commonly used for Agilent logic analyzer probe connections.
Differential I/O Dual 38 Pin	Differential	This connector is commonly used for Agilent logic analyzer probe connections.
Loop Back Test Single Ended IO Dual 40 Pin	Single-ended	0.1 inch spaced header This board serves a dual purpose, in addition to serving as a break-out board for DUT connectivity, it is also used for diagnostic testing.
Single Ended I/O 68 Pin	Single-ended	Single SCSI style connector
Differential I/O Dual 100 Pin	Differential	This connector is commonly used for Agilent logic analyzer probe connections.

The mating connectors for the outputs on the break-out boards are readily available from suppliers external to Agilent Technologies and are listed in Table 3-5 along with the connectors already mounted on the boards.

Table 3-2   **Connector Part Numbers and Manufacturers**

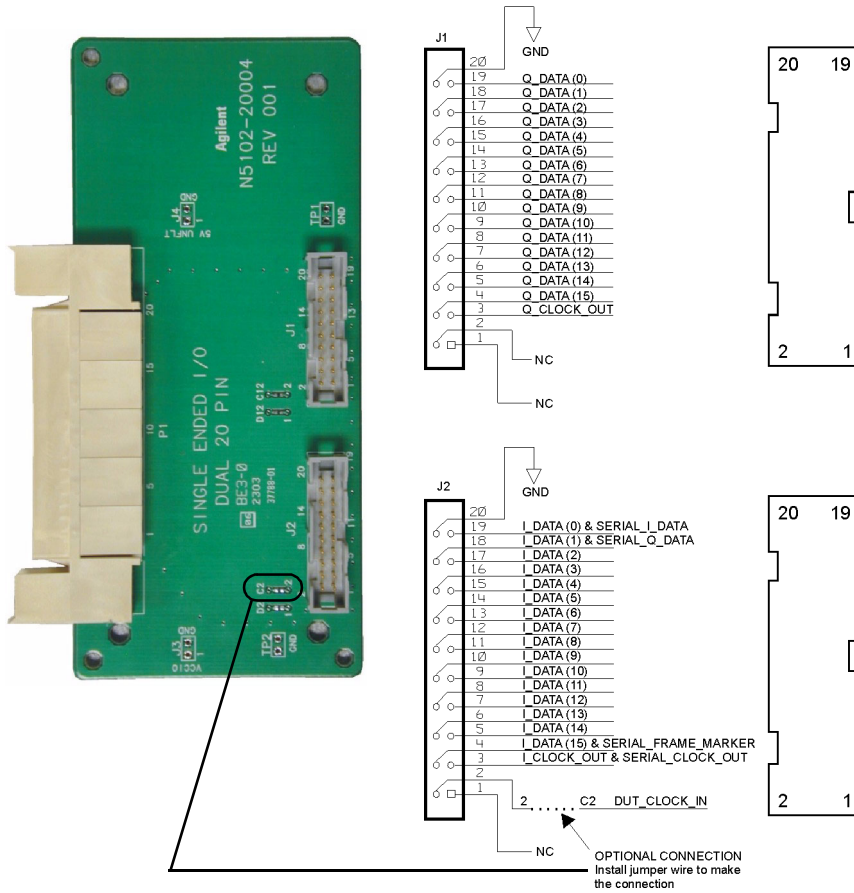| Connector Type	Break-out Board Output Connector Manufacturer Part Number	Mating Connector Manufacturer Part Number	Manufacturer
20-Pin	2520-6002UB	3421-6700 (wire connector)	3M
38-Pin Mictor	2-767004-2	767006-1 (board connector)	Tyco Electronics
40-Pin	2540-6002UB	3417-6700 (wire connector)	3M
68-Pin D-Subminiature	787170-7	749621-7 (wire connector)	Tyco Electronics
100-Pin Samtec	ASP-65067-01	ASP-65267-02 (wire connector)	Samtec

Dual 20-Pin Break-Out Board

Use this break-out board when single-ended testing is required and there are minimal connection points. It is most suitable at lower sample rates using easily constructed ribbon cables. Figure 3-1 shows this board along with the pin-out for the output connectors. The 20-pin connectors are a common 0.1 inch spaced header. You can see in Figure 3-1 that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. Notice that the serial signals are also provided on the J2 connector.

In order for the N5102A module to receive a clock through the Device Interface connector via this break-out board, a jumper wire is required at the 2 to C2 contacts. This is shown in Figure 3-1.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.

**Figure 3-1** **Dual 20-Pin 0.1 Spaced Connector**

Dual 38-Pin Break-Out Board

Figure 3-2 shows this break-out board along with the pin-out for the output connectors. This board is intended for differential testing, however it can also be used for single-ended signals. For single-ended signals, the data is transmitted on the positive lines. Referring to Figure 3-2, notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. The serial signals are also provided on the J2 connector.

In order for the N5102A module to receive a clock through the Device Interface connector via this break-out board, a jumper wire is required at the 2 to C1 contacts for a negative clock and at the 1 to C2 contacts for a positive clock. This is shown in Figure 3-2.

The VCCIO (selected high logic level voltage) is obtained at J4, while the + 5 volt unfiltered DC supply is acquired at J3.

Figure 3-2   Dual 38-Pin Mictor Connector
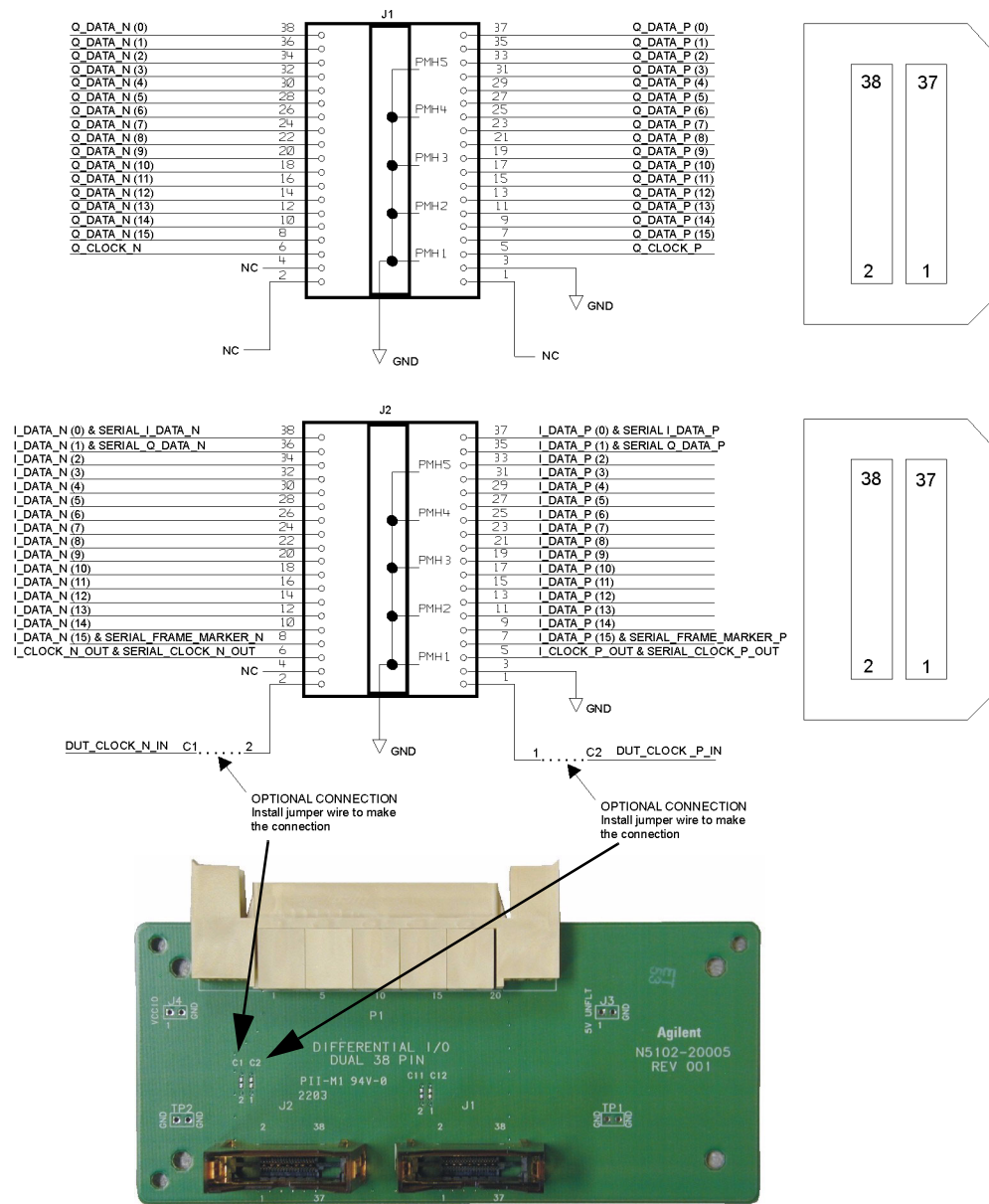
Dual 40 Pin Break-Out Board

This break-out board is useful for higher rate single-ended signals that benefit from a ground associated with each signal line. The 40-pin connectors are a common 0.1 inch spaced header. Figure 3-3 shows this break-out board along with the pin-out for the output connectors. Notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. The serial signals are also provided on the J2 connector.

This board serves a dual function, one as a break-out board simplifying the connectivity of the DUT and the other as a loop back test board when performing a diagnostic test.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.
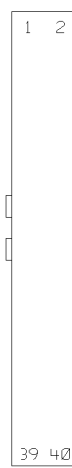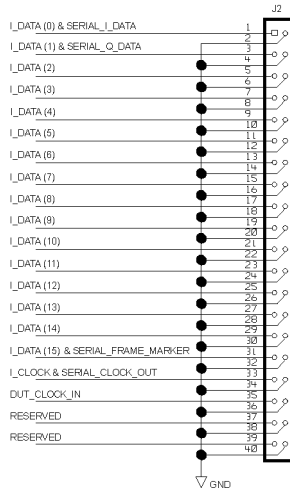
Figure 3-3   **Dual 40 Pin 0.1 Spaced Header Connectors**
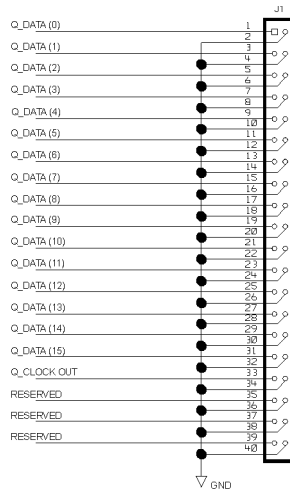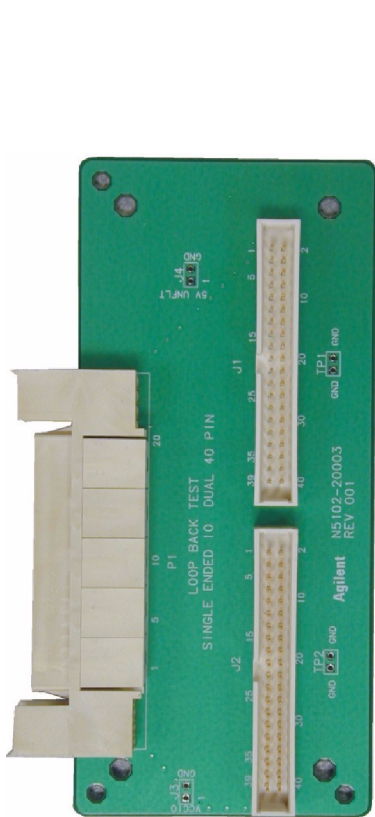
Single 68-Pin SCSI Style Break-Out Board

Figure 3-4 shows this break-out board along with the pin-out for the output connector. This break-out board is intended for single-ended testing. The output connector is a SCSI style interface that is compatible with some existing products that provide a digital data output. The serial signals are transmitted on the I data lines.

In order for the N5102A module to receive a clock through the Device Interface connector via this break-out board, a jumper wire is required at the 66 to C2 contacts. This is shown in Figure 3-4.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.

Figure 3-4　　　　　　　**Single 68-Pin D-Subminiature SCSI Style Connector**
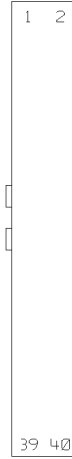
Dual 100-Pin Break-Out Board

Figure 3-5 shows this break-out board along with the pin-out for the output connectors. It is intended for differential testing, however it can also be used for single-ended signals. For single-ended signals, the data is transmitted on the positive lines. You can see in Figure 3-5 that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. Notice that the serial signals are also provided on the J2 connector.

The VCCIO (selected high logic level voltage) is obtained at J4, while the + 5 volt unfiltered DC supply is acquired at J3.

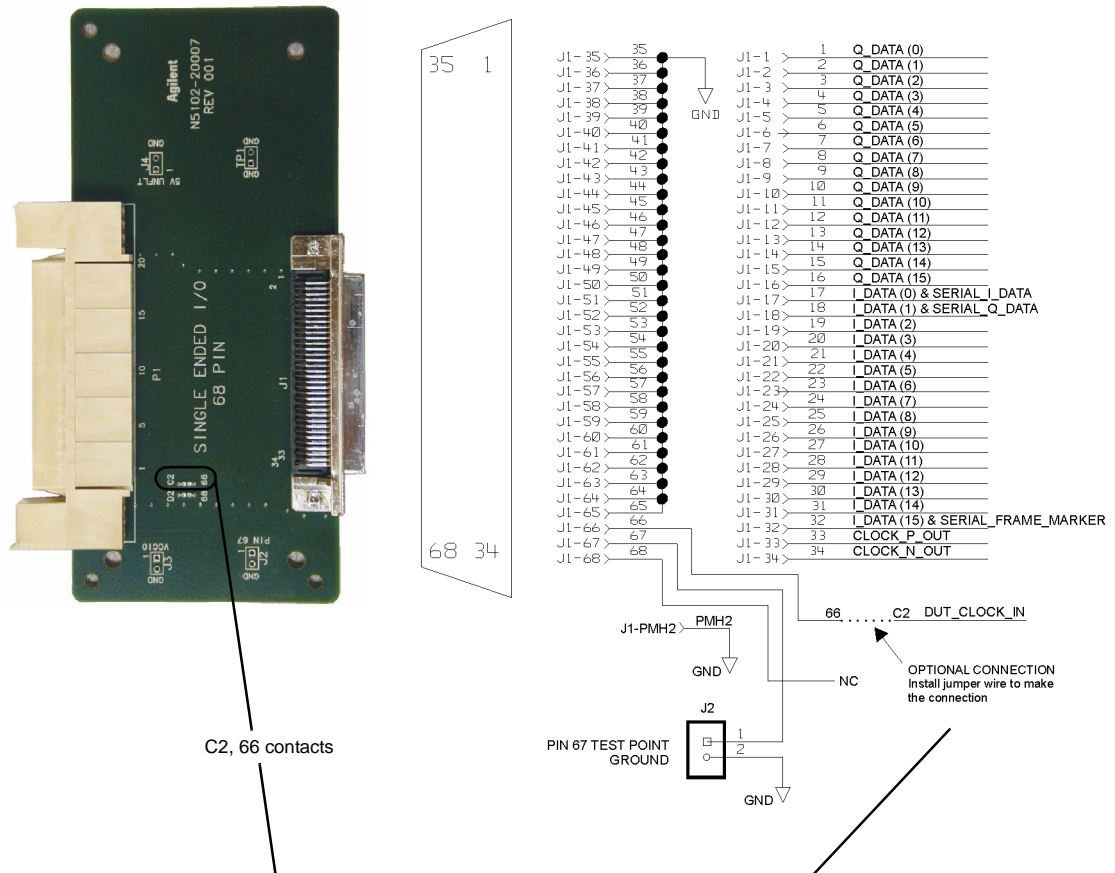**Figure 3-5**   **Dual 100-Pin Samtec Connector**
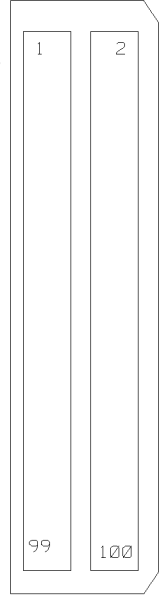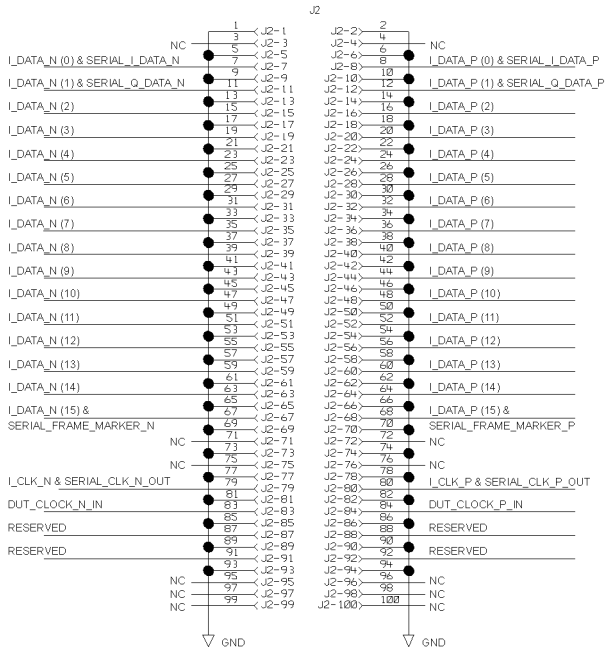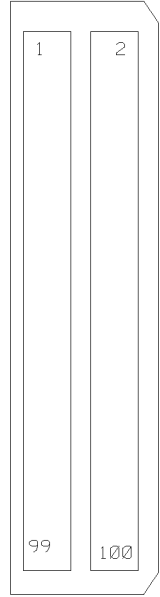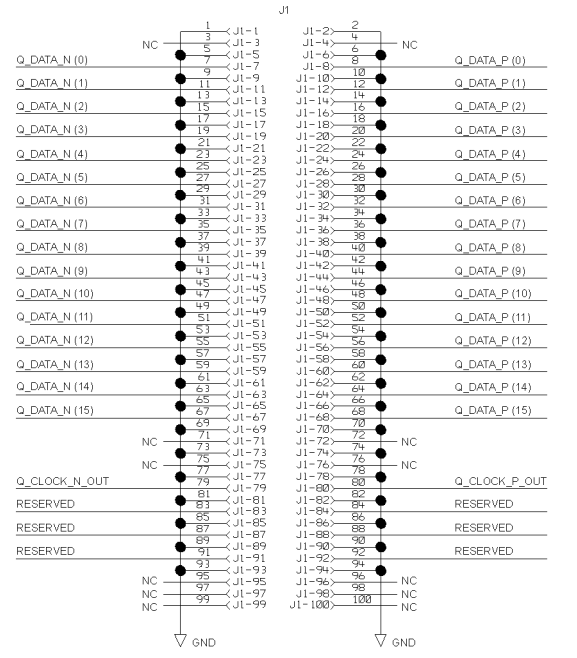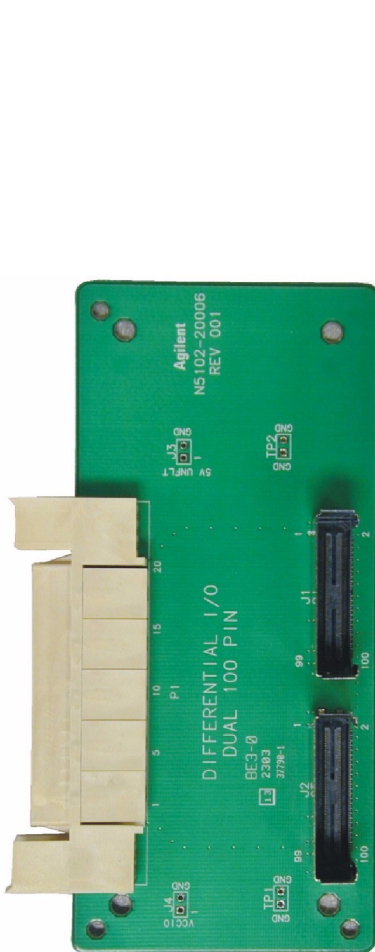
Device Interface Connector

The figures and information shown in this section will facilitate customizing a connection solution for your DUT using the supplied device interface mating connector (see "Device Interface Mating Connector" on page 39). The signal contact layout for the Device Interface connector is shown in Figure 3-6 and the connector pin-out is shown in Figure 3-7 and Figure 3-8.

Figure 3-6   Device Interface Connector Layout
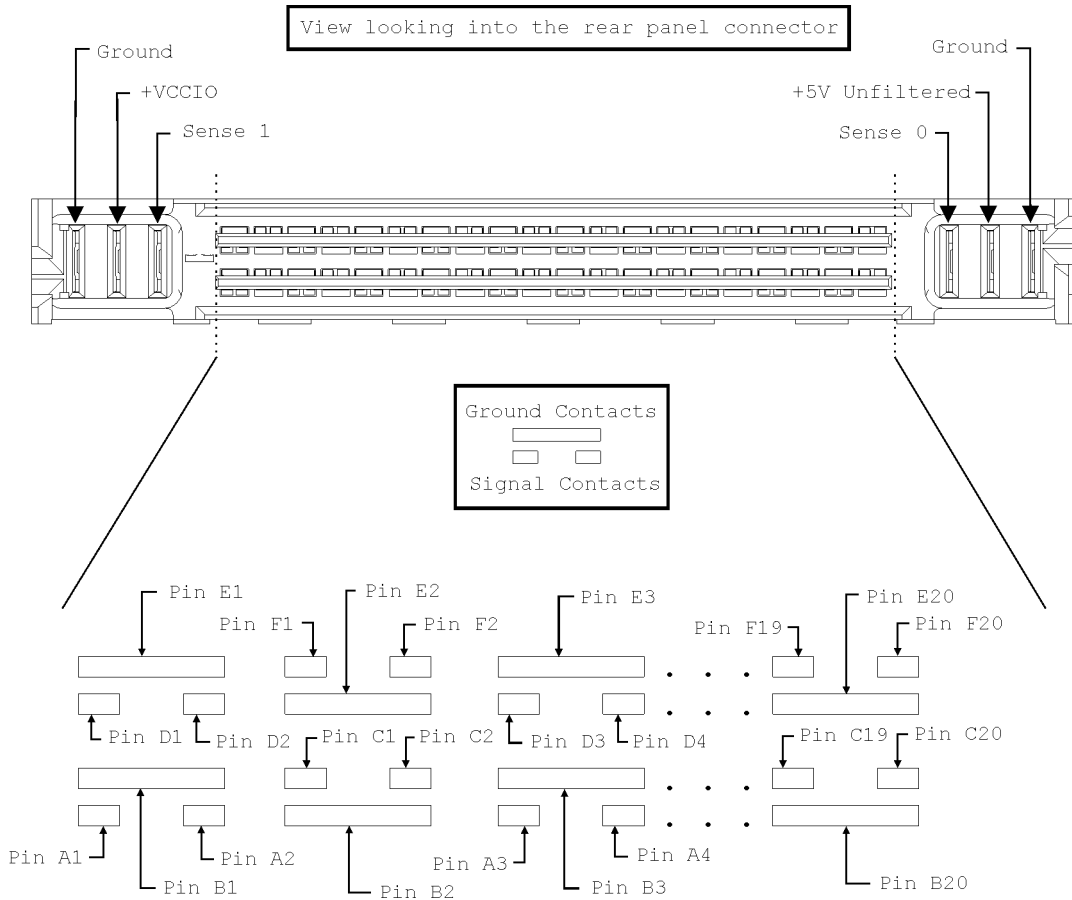
Figure 3-7 **Device Interface Connector Pin-Out**

W1 X1 Y1 Z1 ← GND

W2 X2 Y2 Z2 ← +5V UNFILTERED

W3 X3 Y3 Z3 ← SENSE (0)

C20 ← Q_DATA_P (1)	F20 ← Q_DATA_P (0)
C19 ← Q_DATA_N (1)	F19 ← Q_DATA_N (0)
B20 ← GND	E20 ← GND
A20 ← Q_DATA_P (3)	D20 ← Q_DATA_P (2)
A19 ← Q_DATA_N (3)	D19 ← Q_DATA_N (2)
B19 ← GND	E19 ← GND
C18 ← Q_DATA_P (5)	F18 ← Q_DATA_P (4)
C17 ← Q_DATA_N (5)	F17 ← Q_DATA_N (4)
B18 ← GND	E18 ← GND
A18 ← Q_DATA_P (7)	D18 ← Q_DATA_P (6)
A17 ← Q_DATA_N (7)	D17 ← Q_DATA_N (6)
B17 ← GND	E17 ← GND
C16 ← Q_DATA_P (9)	F16 ← Q_DATA_P (8)
C15 ← Q_DATA_N (9)	F15 ← Q_DATA_N (8)
B16 ← GND	E16 ← GND
A16 ← Q_DATA_P (11)	D16 ← Q_DATA_P (10)
A15 ← Q_DATA_N (11)	D15 ← Q_DATA_N (10)
B15 ← GND	E15 ← GND
C14 ← Q_DATA_P (13)	F14 ← Q_DATA_P (12)
C13 ← Q_DATA_N (13)	F13 ← Q_DATA_N (12)
B14 ← GND	E14 ← GND
A14 ← Q_DATA_P (15)	D14 ← Q_DATA_P (14)
A13 ← Q_DATA_N (15)	D13 ← Q_DATA_N (14)
B13 ← GND	E13 ← GND
C12 ← RESERVED	F12 ← Q_CLOCK_P
C11 ← RESERVED	F11 ← Q_CLOCK_N
B12 ← GND	E12 ← GND
A12 ← RESERVED	D12 ← RESERVED
A11 ← RESERVED	D11 ← RESERVED
B11 ← GND	E11 ← GND

Figure 3-8   Device Interface Connector Pin-Out (continued)

```
C10 ←————— I_DATA_P (1) & SERIAL_Q_DATA_P          F10 ←————— I_DATA_P (0) & SERIAL_I_DATA_P
C9  ←————— I_DATA_N (1) & SERIAL_Q_DATA_N          F9  ←————— I_DATA_N (0) & SERIAL_I_DATA_N
B10 ←———————————————— GND                          E10 ←———————————————— GND
A10 ←————— I_DATA_P (3)                             D10 ←————— I_DATA_P (2)
A9  ←————— I_DATA_N (3)                             D9  ←————— I_DATA_N (2)
B9  ←———————————————— GND                           E9  ←———————————————— GND
C8  ←————— I_DATA_P (5)                             F8  ←————— I_DATA_P (4)
C7  ←————— I_DATA_N (5)                             F7  ←————— I_DATA_N (4)
B8  ←———————————————— GND                           E8  ←———————————————— GND
A8  ←————— I_DATA_P (7)                             D8  ←————— I_DATA_P (6)
A7  ←————— I_DATA_N (7)                             D7  ←————— I_DATA_N (6)
B7  ←———————————————— GND                           E7  ←———————————————— GND
C6  ←————— I_DATA_P (9)                             F6  ←————— I_DATA_P (8)
C5  ←————— I_DATA_N (9)                             F5  ←————— I_DATA_N (8)
B6  ←———————————————— GND                           E6  ←———————————————— GND
A6  ←————— I_DATA_P (11)                            D6  ←————— I_DATA_P (10)
A5  ←————— I_DATA_N (11)                            D5  ←————— I_DATA_N (10)
B5  ←———————————————— GND                           E5  ←———————————————— GND
C4  ←————— I_DATA_N (13)                            F4  ←————— I_DATA_P (12)
C3  ←————— I_DATA_N (13)                            F3  ←————— I_DATA_N (12)
B4  ←———————————————— GND                           E4  ←———————————————— GND
A4  ←————— I_DATA_P (15) & SERIAL_FRAME_MARKER _P   D4  ←————— I_DATA_P (14)
A3  ←————— I_DATA_N (15) & SERIAL_FRAME_MARKER_N    D3  ←————— I_DATA_N (14)
B3  ←———————————————— GND                           E3  ←———————————————— GND
C2  ←————— DUT_CLOCK_IN_P                           F2  ←————— I_CLOCK_P & SERIAL_CLOCK_P_OUT
C1  ←————— DUT_CLOCK_IN_N                           F1  ←————— I_CLOCK_N & SERIAL_CLOCK_N_OUT
B2  ←———————————————— GND                           E2  ←———————————————— GND
A2  ←————— RESERVED                                 D2  ←————— RESERVED
A1  ←————— RESERVED                                 D1  ←————— RESERVED
B1  ←———————————————— GND                           E1  ←———————————————— GND

W4 X4 Y4 Z4  ←————————————————— SENSE (1)

W5 X5 Y5 Z5  ←————————————————— +VCCIO

W6 X6 Y6 Z6  ←————————————————— GND
```

Input and Output Clock Signals

There are multiple output clock lines and two input clock lines to handle differential clocking. The N5102A module can be configured to accept the DUT clock through the Device Interface connector for data clocking. Using the input clock signal from the Device Interface connector is an alternative to using a clock signal applied to the Clock In connector. Table 3-3 lists the Device Interface connector pins for the different clock signals and the serial frame marker.

Table 3-3   Clock Signal and Serial Frame Marker Lines

Clock Signal Type	Pin
Output Q-Clock Pos	F12
Output Q-Clock Neg	F11
Output I-Clock Pos	F2
Output I-Clock Neg	F1
Output Serial Clock Pos	F2
Output Serial Clock Neg	F1
Output Serial Frame Marker Pos	A4
Output Serial Frame Marker Neg	A3
Input Clock Signal (DUT Clock) Pos	C2
Input Clock Signal (DUT Clock) Neg	C1

Data Lines

There are 64 data lines on the Device Interface connector that allow for either differential or single-ended signals. These 64 data lines consist of 32-I lines (16 positive and 16 negative), and 32-Q lines (16 positive and 16 negative). Single-ended signals are routed on the positive data lines. Table 3-4 shows which data lines are used for a given signal.

Table 3-4   Data Lines

Signal	Serial Data		Parallel Data[1]	
	I	Q	I	Q
Differential	Positive and negative lines: F9 & F10	Positive and negative lines: C9 & C10	Positive and negative lines 0–16 (A3–A10, C3–C10 D3–D10, F3–F10)	Positive and negative lines 0–16 (A13–A20, C13–C20, D13–D20, F13–F20)
Single-Ended	F10	C10	Positive lines 0–16 (A4, A6, A8, A10, C4, C6, C8, C10, D4, D6, D8, D10, F4, F6, F8, F10)	Positive lines 0–16 (A14, A16, A18, A20, C14, C16, C18, C20, D14, D16, D18, D20, F14, F16, F18, F20)

1. Parallel interleaving (IQ and QI) occurs on the I data lines.

DC Supply

Referring to Figure 3-6, you can see that the interface module provides an unfiltered +5 volts DC supply through the Device Interface connector. This DC supply provides up to 100 mA and has a self-resettable fuse. You can use this DC current to bias components on the DUT where the noise will not compromise test results.

VCCIO

The Device Interface connector also provides a connection for the VCCIO that can be measured at a test point on each break-out board. The VCCIO amplitude is equal to the high voltage level of the selected logic type.

Device Interface Mating Connector

A mating connector for the Device Interface port is supplied to facilitate the DUT connection when none of the break-out boards provide a connection solution for your DUT.

There are two ways to use the mating connector. One is to attach wires directly to the pins providing a quick connection solution. The other is to make a PC board with a footprint that matches the connector mounting pins. Figure 3-9 shows the layout of the signal contacts while looking directly into the connector and the pin footprint while viewing the connector from the bottom, and Figure 3-10 shows the connector footprint for a PC board.

The signal pin-out for the connector can be obtained from Figure 3-7 on page 35 and Figure 3-8 on page 36. These figures display the pin-out for the N5102A module Device Interface connector.

Table 3-5 provides the manufacturer and the part numbers for the Device Interface connector and its mate. Both connectors are readily available from suppliers external to Agilent Technologies.

Table 3-5

Connector Type	Connector Manufacturer Part Number	Mating Connector Manufacturer Part Number	Manufacturer
144-Pin Z-Dok+	1367550-5	1367555-2 (board connector)	Tyco Electronics

Figure 3-9   Z-Dok+ Device Interface Mating Connector Layout and Footprint

Figure 3-10   Z-Dok+ Device Interface Mating Connector PC Board Foot Print

Component Side Shown

It is recommended that you check the Tyco Electronics
web site for the most current PC board footprint drawing.

Rows A, C, D, and F are signal contacts. Rows B and E are ground contacts.

4 DIMENSIONS PER CUSTOMER BOARD LAYOUT.

DUT Connections
Device Interface Mating Connector
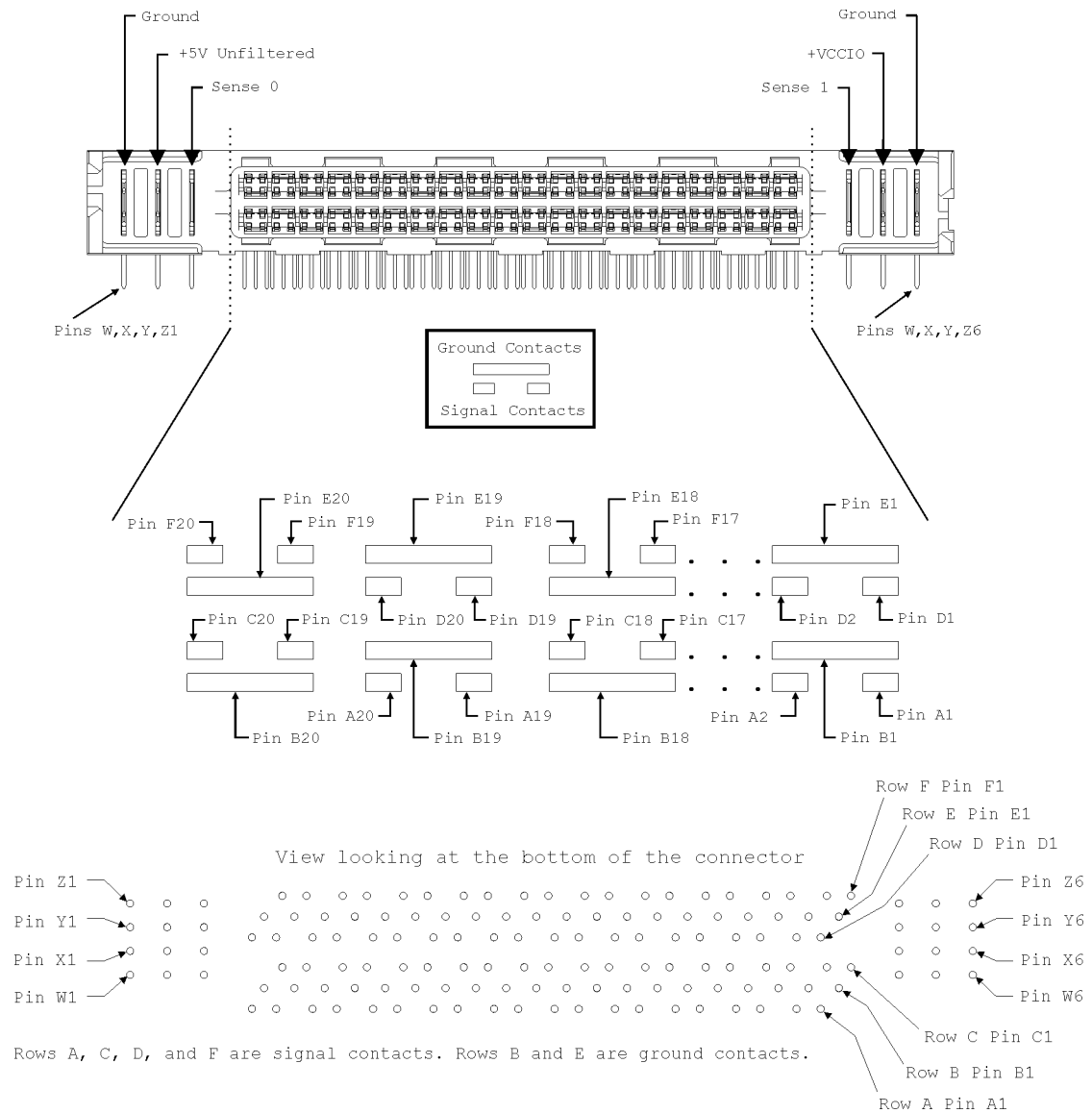
4   Operation

This chapter provides N5102A Baseband Studio digital signal interface module clock timing information and will guide you through configuring the digital signal parameters.

Clock Timing

This section describes how clocking for the digital data is provided. Clock timing information and diagrams are supplied for the different port configurations (serial, parallel, or parallel interleaved data transmission) and phase and skew settings. All settings for the interface module are accomplished using the signal generator UI.

Clock and Sample Rates

The clock is the signal that tells when the bits of a sample are valid. (A sample is a group of bits where the size of the sample is set using the Word Size softkey). The clock and sample rates are displayed in the first-level and data setup softkey menus for the N5102A module UI.

Figure 4-1   Data Setup Menu for a Parallel Port Configuration
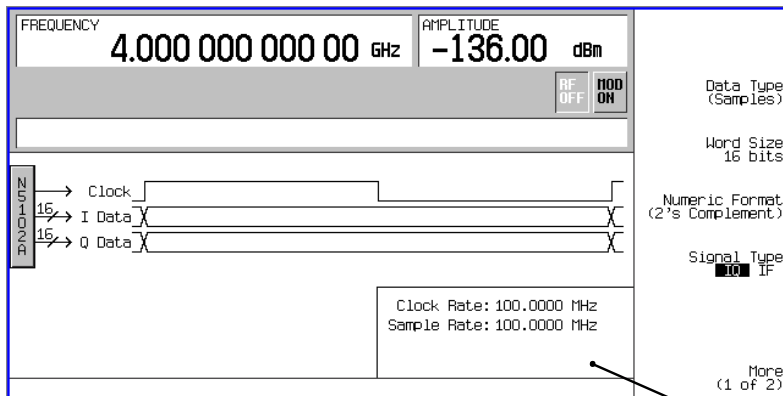
Clock and sample rates

The N5102A module clock rate is set using the **Clock Rate** softkey and has a maximum range of 1 kHz to 400 MHz. The sample rate is automatically calculated and has a maximum range of 1 kHz to 100 MHz. These ranges can be smaller depending on:

- logic type
- data parameters
- clock configuration

Logic Type Output Levels

The N5102A module maximum clock rate is dependent on the logic and signal type. However not all logic

type output levels are maintained to the maximum clock rate. Table 4-1 shows the warranted logic type output level clock rates and maximum clock rates for the logic and signal types. Notice that LVDS using an IF signal is the only logic type where the warranted and maximum rates are the same.

Table 4-1   **Warranted Output Level Clock Rates and Maximum Clock Rates**

Logic Type	Warranted Output Level Clock Rates		Maximum Clock Rates	
	IQ Signal Type	IF Signal Type[1]	IQ Signal Type	IF Signal Type
LVTTL and CMOS	100 MHz	100 MHz	150 MHz	150 MHz
LVDS	200 MHz	400 MHz	300 MHz	400 MHz

1. The IF signal type is not available for a serial port configuration.

The output levels will degrade above the warranted output level clock rates, but they may still be usable.

Serial Port Configuration Clock and Sample Rates

For a serial port configuration, the lower clock rate limit is determined by the word size (word size and sample size are synonymous), while the maximum clock rate limit remains constant at 150 MHz for LVTTL and CMOS logic types, and 300 MHz for an LVDS logic type.

The reverse is true for the sample rate. The lower sample rate value of 1 kHz remains while the upper limit of the sample rate varies with the word size. For example, a five-bit sample for an LVTTL or CMOS logic type yields the following range values:

- Clock rate of 5 kHz to 150 Mhz
- Sample rate of 1 kHz to 30 MHz

Since a five-bit sample was used, a factor of five is used to calculate the minimum clock rate (5-bits x 1 kHz) and the maximum sample rate (150 MHz clock rate / 5-bits). Table 4-2 shows the serial clock and sample rate ranges for each word size.

Table 4-2 **Serial Port Configuration Maximum Clock and Sample Rates**

Word Size (Bits)	Logic Type: LVTTL and CMOS		Logic Type: LVDS	
	Clock Rate Range	Sample Rate Range	Clock Rate Range	Sample Rate Range
4	4 kHz–150 MHz	1 kHz–37.5 MHz	4 kHz–300 MHz	1 kHz–75 MHz
5	5 kHz–150 MHz	1 kHz–30 MHz	5 kHz–300 MHz	1 kHz–60 MHz
6	6 kHz–150 MHz	1 kHz–25 MHz	6 kHz–300 MHz	1 kHz–50 MHz
7	7 kHz–150 MHz	1 kHz–21.4286 MHz	7 kHz–300 MHz	1 kHz–42.8571 MHz
8	8 kHz–150 MHz	1 kHz–18.75 MHz	8 kHz–300 MHz	1 kHz–37.5 MHz
9	9 kHz–150 MHz	1 kHz–16.6667 MHz	9 kHz–300 MHz	1 kHz–33.3333 MHz
10	10 kHz–150 MHz	1 kHz–15 MHz	10 kHz–300 MHz	1 kHz–30 MHz
11	11 kHz–150 MHz	1 kHz–13.6364 MHz	11 kHz–300 MHz	1 kHz–27.2727 MHz
12	12 kHz–150 MHz	1 kHz–12.5 MHz	12 kHz–300 MHz	1 kHz–25 MHz
13	13 kHz–150 MHz	1 kHz–11.5385 MHz	13 kHz–150 MHz	1 kHz–23.0769 MHz
14	14 kHz–150 MHz	1 kHz–10.7143 MHz	14 kHz–300 MHz	1 kHz–21.4286 MHz
15	15 kHz–150 MHz	1 kHz–10 MHz	15 kHz–300 MHz	1 kHz–20 MHz
16	16 kHz–150 MHz	1 kHz–9.375 MHz	16 kHz–300 MHz	1 kHz–18.75 MHz

Parallel and Parallel Interleaved Port Configuration Clock and Sample Rates

Parallel and parallel interleaved port configurations have other limiting factors for the clock and sample rate ranges:

- logic type
- Clocks per sample selection
- IQ or IF digital signal type

Clocks per sample is the ratio of the clock to sample rate. For an IQ signal type, the sample rate is reduced by the clocks per sample value when the value is greater than one. For an IF signal, clocks per sample is always set to one. Table 4-3 shows the parallel and parallel interleaved port configuration clock and sample rates.

Table 4-3   **Parallel and Parallel Interleaved Maximum Signal Ranges**

Clocks Per Sample	Signal Type	Logic Type: LVTTL and CMOS		Logic Type: LVDS	
		Clock Rate Range	Sample Rate Range	Clock Rate Range	Sample Rate Range
1	IQ	1 kHz–100 MHz	1 kHz–100 MHz	1 kHz–100 MHz	1 kHz–100 MHz
2		2 kHz–150 MHz	1 kHz–75 MHz	2 kHz–200 MHz	1 kHz–100 MHz
4		4 kHz–150 MHz	1 kHz–37.5 MHz	4 kHz–300 MHz	1 kHz–75 MHz
1	IF	4 kHz–150 MHz	4 kHz–150 MHz	4 kHz–400 MHz	4 kHz–400 MHz

Clock Source

The clock signal for the N5102A module is provided in one of three ways:

- generated internally to the interface module
- provided externally via the Ext Clock In connector
- provided externally via the Device Interface connector

The clock source selection is accomplished using the N5102A module UI on the signal generator, see Figure 4-2.

Figure 4-2   **Clock Source Selection**
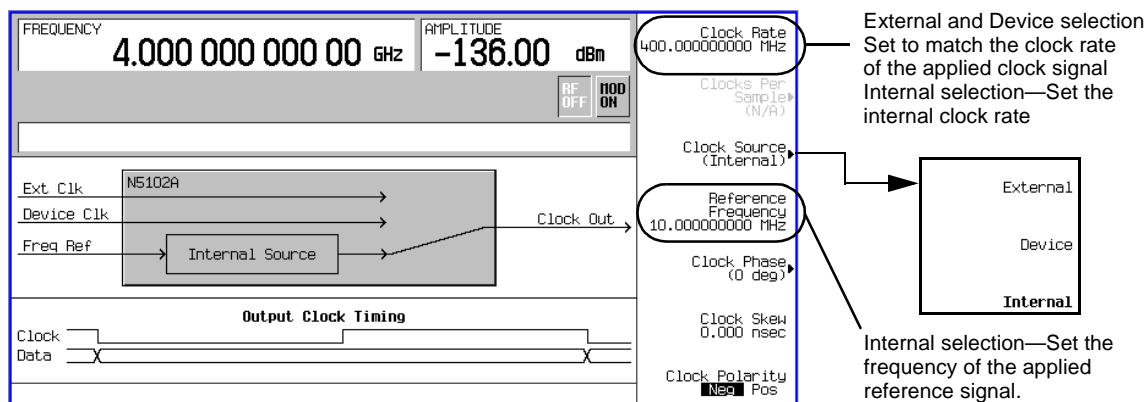
When you select a clock source, you must let the N5102A module know the frequency of the clock signal using the **Clock Rate** softkey. When internal is the clock selection, this softkey sets the internal clock rate; for

the Device and External selections, this softkey must reflect the frequency of the applied clock signal.

When Internal is the clock source selection, a frequency reference is applied to the Freq Ref connector. The frequency of this applied signal needs to be entered using the **Reference Frequency** softkey, unless the current setting matches that of the applied signal.

Table 4-4 shows the clock source selections and the connector that accepts the externally applied signal along with the required softkey setting for each selection.

Table 4-4 **Clock Source Settings and Connectors**

Clock Source	Softkeys		N5102A Module Connection		
	Reference Frequency	Clock Rate[1]	Freq Ref	Ext Clock In	Device Interface
External		●		●	
Device		●			●
Internal[2]	●	●	●		

1. For the Internal selection, this sets the internal clock rate. For the External and Device selections, this tells the interface module the rate of the applied clock signal.
2. There should be no clock signal applied to the Ext Clock In connector.

The selected clock source provides the interface module output clock signal at the Clock Out and the Device Interface connectors.

Common Frequency Reference

The clocking flexibility of the digital signal interface module allows the setting of arbitrary clock rates for the DUT. In general, the clock rate inside the ESG/PSG will be different from the interface module clock rate, so the interface module performs a rate conversion for clocking the data that is transmitted to the DUT. An important aspect of this conversion is to have accurate clock rate information to avoid loosing data. The module relies on relative clock accuracy, instead of absolute accuracy, that must be ensured by using a single frequency reference that is common to all clock rates involved in the test setup. This can be implemented in various ways (see the five drawings in Figure 4-3 on page 50), but whatever way it is implemented, the clock inside the signal generator must have the same base frequency reference as the clock used by the DUT.

When a frequency reference is connected to the signal generator, it is applied to one of two rear panel connectors:

- 10 MHz IN
- BASEBAND GEN REF IN

The BASEBAND GEN REF IN connector will accept a frequency reference in the range of 1 to 100 MHz. In the situations where the external or DUT clock source can neither provide or accept a frequency reference, their clock signal can be applied to this same connector and used as the frequency reference.

Whenever an external clock signal or frequency reference is connected to the BASEBAND GEN REF IN connector, the frequency of the clock signal or the frequency reference needs to be entered into the signal generator modulation format being used. For information on the BASEBAND GEN REF IN connector for the ESG, refer to the *Agilent ESG Vector Signal Generator User's Guide*, and for the PSG, refer to the *Agilent PSG Signal Generators User's Guide*. For information on the associated softkeys and fields for entering the frequency of the applied clock signal or frequency reference, refer to the *Agilent ESG Vector Signal Generator Key and Data Field Reference* or the *Agilent PSG Signal Generators Key Reference* according to the signal generator being used.

Figure 4-3 **Frequency Reference Setup Diagrams for the N5102A Module Clock Signal**

Internally Generated Clock

Device (DUT) Supplied Clock
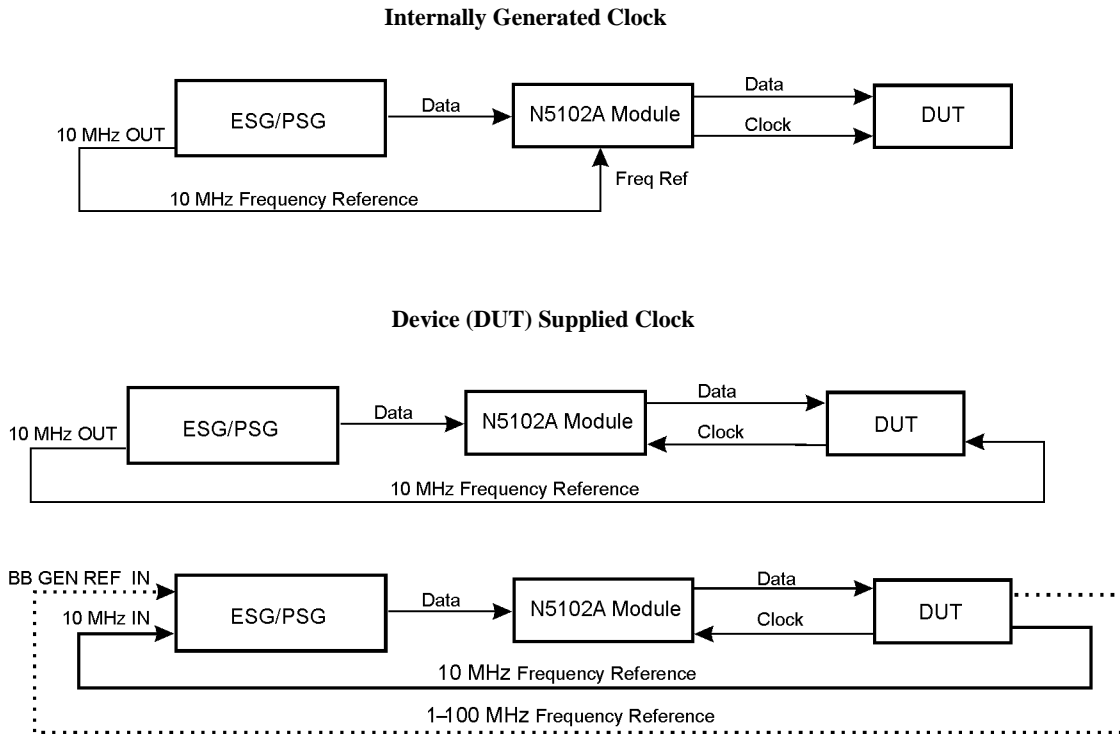
NOTE: Use only one of the two signal generator frequency reference inputs.

Externally Supplied Clock
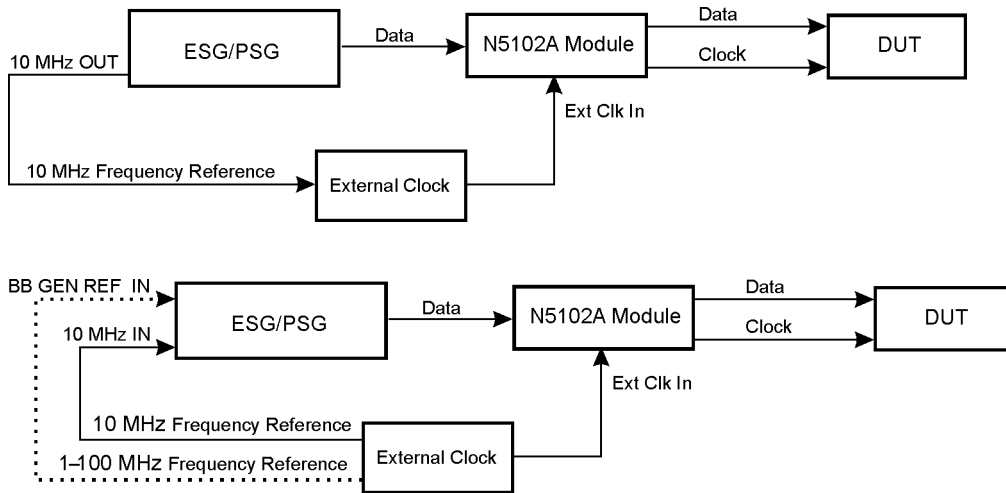
NOTE: Use only one of the two signal generator frequency reference inputs.

Clock Timing for Parallel Data

Some components require multiple clocks during a single sample period. (A sample period consists of an I and Q sample, and both are transmitted during a sample period). For parallel data transmissions, you have the option of selecting one, two, or four clocks per sample. For clocks per sample greater than one, the I and Q samples are held to accommodate the additional clock periods. This reduces the sample rate relative to the clock rate by a factor equal to the clocks per sample selection. For example, when four is selected, the sample rate is reduced by a factor of four (sample rate to clock rate ratio). Figure 4-4 demonstrates the clock timing for each clocks per sample selection.

Figure 4-4   Clock Sample Timing for Parallel Port Configuration

2 Clocks Per Sample

Sample rate decreases by a factor of two

1 Sample Period
2 Clocks

Clock

I sample
4 bits per word

0	0	0
1	1	1
2	2	2
3	3	3

Q sample
4 bits per word

0	0	0
1	1	1
2	2	2
3	3	3

4 Clocks Per Sample

Sample rate decreases by a factor of four

1 Sample Period
4 Clocks

Clock

I sample
4 bits per word

0	0
1	1
2	2
3	3

Q sample
4 bits per word

0	0
1	1
2	2
3	3
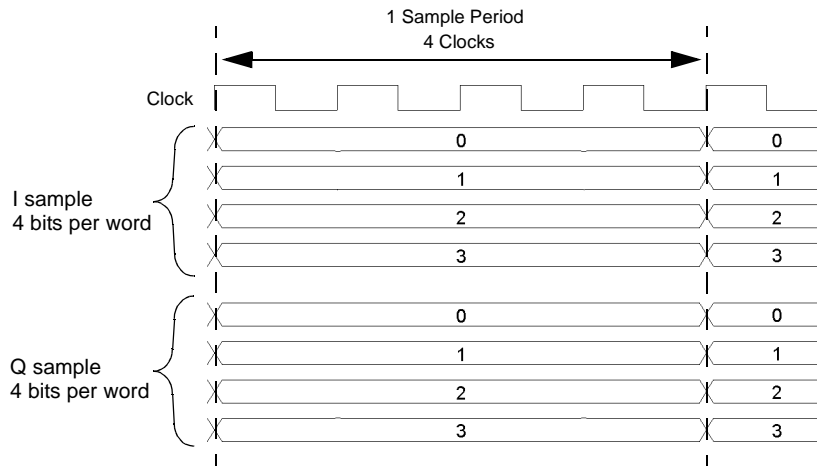
Clock Timing for Parallel Interleaved Data

The N5102A module provides the capability to interleave the digital I and Q samples. There are two choices for interleaving, IQ where the I sample is transmitted first and QI where the Q sample is transmitted first. When parallel interleaved is selected, all samples are transmitted on the I data lines. This effectively transmits the same number of samples during a sample period on half the number of data lines as compared to non-interleaved samples. (A sample period consists of an I and Q sample, and both are transmitted during a sample period.) Clocks per sample is still a valid parameter for parallel interleaved transmissions and creates a reduction in the sample rate relative to the clock rate. The clocks per sample selection is the ratio of the reduction. Figure 4-5 shows each of the clocks per sample selections for a parallel IQ interleaved port configuration and the clock timing relative to the I and Q samples. For a parallel QI interleaved port configuration, just reverse the I and Q sample positions.

Figure 4-5   **Clock Timing for a Parallel IQ Interleaved Port Configuration**

1 Clock Per Sample

The I sample is transmitted on one clock transition and the Q sample is transmitted on the other transition; the sample and clock rates are the same.
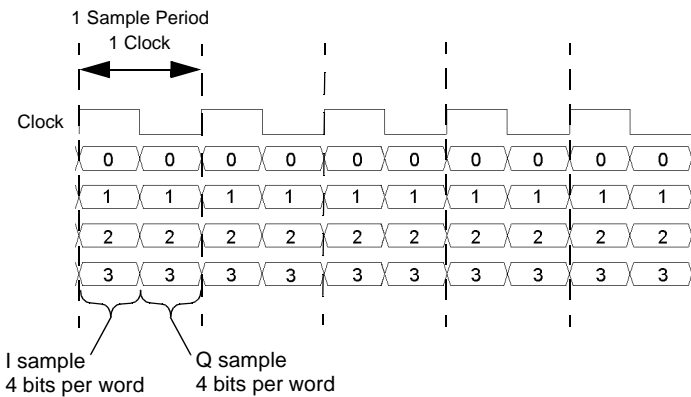
2 Clocks Per Sample

The I sample is transmitted for one clock period and the Q sample is transmitted during the second clock period; the sample rate decreases by a factor of two.
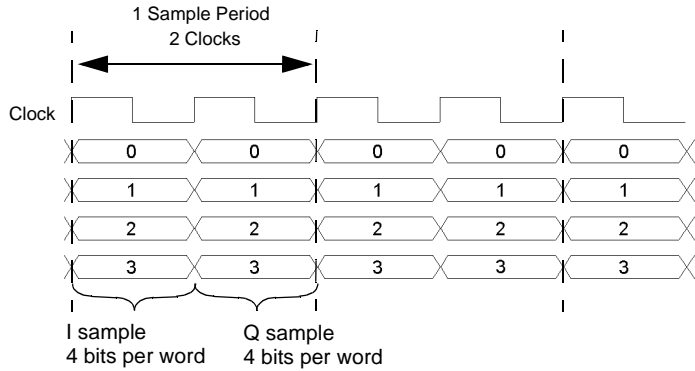
4 Clocks Per Sample

The I sample is transmitted for the first two clock periods and the Q sample is transmitted during the second two clock periods; the sample rate is decreased by a factor of four.
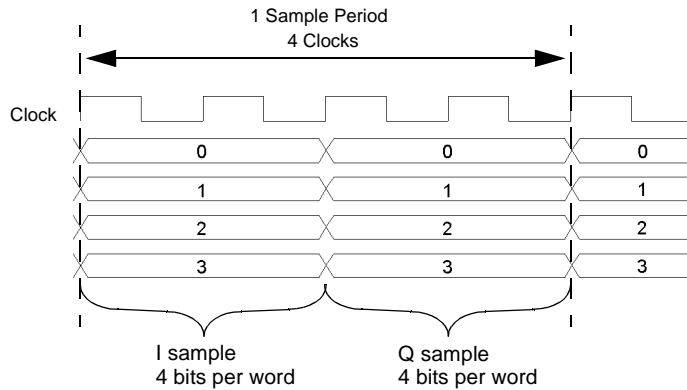
Clock Timing for Serial Data

Figure 4-6 shows the clock timing for a serial port configuration. Notice that the serial transmission includes frame pulses that mark the beginning of each sample where the clock delineates the beginning of each bit. For a serial transmission, the clock and the bit rates are the same, but the sample rate varies depending on the number of bits per word that are entered using the **Word Size** softkey. The number of bits per word is the same as the number of bits per sample.

Figure 4-6   Clock Timing for a Serial Port Configuration
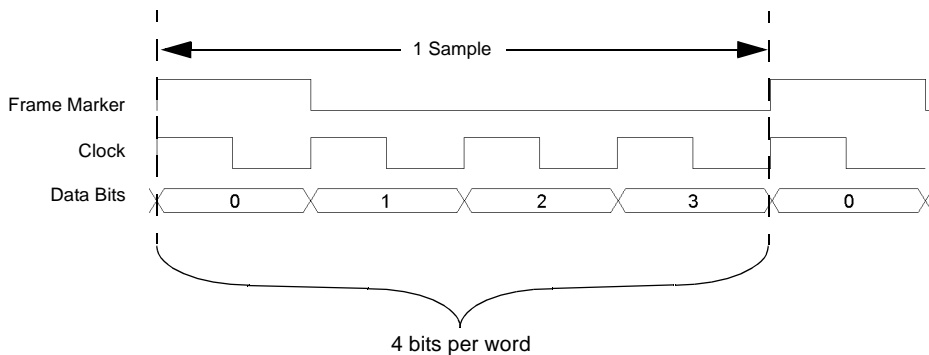
Clock Timing for Phase and Skew Adjustments

The N5102A module provides phase and skew adjustments for the clock relative to the data and can be used to align the clock with the valid portion of the data. The phase has a 90 degree resolution (0, 90, 180, and 270 degree selections) for clock rates from 10 to 200 MHz and a 180 degree resolution (0 and 180 degree selections) for clock rates below 10 MHz and greater than 200 MHz.

The skew is displayed in nanoseconds with a maximum range of ±5 ns using a maximum of ±127 discrete steps. Both the skew range and the number of discrete steps are variable with a dependency on the clock rate. The skew range contracts as the clock rate is increased and expands as the clock rate is decreased. The maximum skew range is reached at a clock rate of approximately 99 MHz and is maintained down to a clock rate of 25 MHz. For clock rates below 25 MHz, the skew adjustment is unavailable.

A discrete step is the resolution between each skew range value and is calculated using the formula:

$$\frac{1}{256 \times \text{Clock Rate}}$$

The number of discrete steps required to reach the maximum skew range decreases at lower frequencies. For example, at a clock rate of 50 MHz, 127 steps would exceed the maximum skew range of ±5 ns, so the actual number of discrete steps would be less than 127.

Figure 4-7 is an example of a phase and skew adjustment and shows the original clock and its phase position relative to the data after each adjustment. Notice that the skew adjustment adds to the phase setting.

Figure 4-7   **Clock Phase and Skew Adjustments**
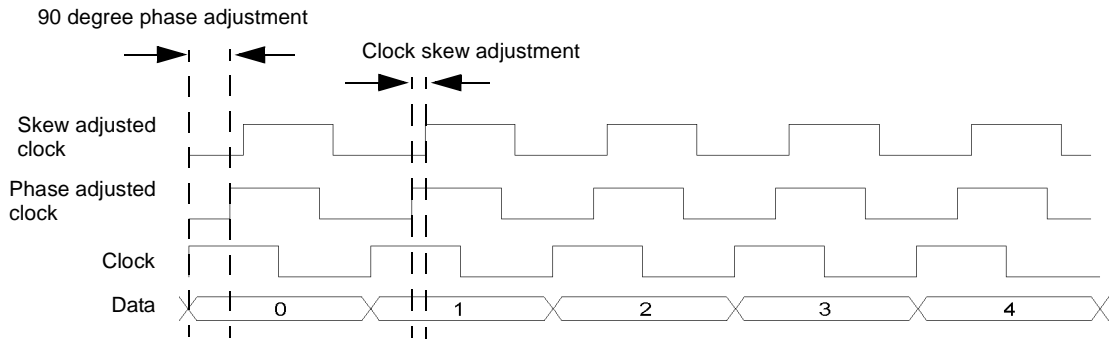
Connecting the Clock Source and DUT

As shown in Figure 4-3 on page 50, there are numerous ways to provide a common frequency reference to the system components (ESG/PSG, N5102A module, and the DUT). Figure 4-8 shows an example setup where the signal generator supplies the common frequency reference and the N5102A module is providing the clock to the DUT.

CAUTION   The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

Figure 4-8   **Example Setup using the ESG/PSG 10 MHz Frequency Reference**

Signal generator 10 MHz Out

Freq Ref connector

Break-out board

DUT

Device interface connection

User furnished ribbon cable(s) connect between DUT and break-out board
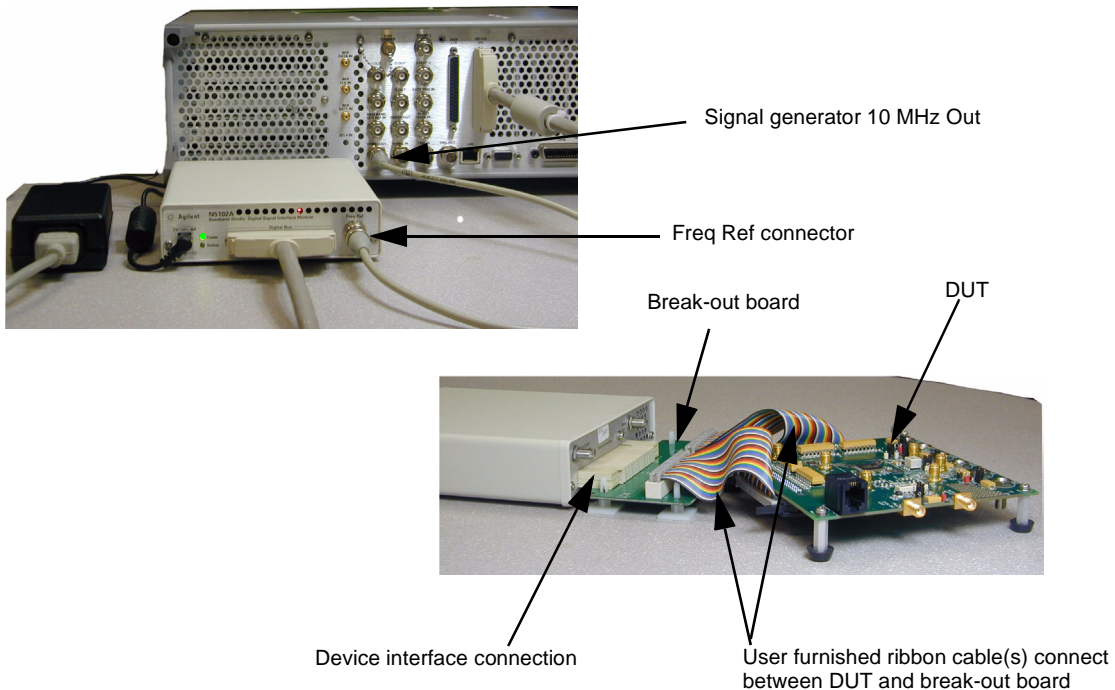
1. Refer to the five setup diagrams in Figure 4-3 on page 50 and connect the frequency reference cable according to the clock source.

2. If an external clock source is used, connect the external clock signal to the Ext Clock In connector on the interface module.

3. If the DUT incorporates the Device Interface mating connector, refer to Figure 4-8 for the device

interface connection and connect the DUT to the Device Interface connector on the N5102A module. Then proceed to "Operating the N5102A Module" on page 60.

4. If the DUT does not incorporate the Device Interface mating connector, select the break-out board that contains the output connector suited for your application.

5. Refer to Figure 4-8 and connect the break-out board to the Device Interface connector on the N5102A module.

6. Connect the DUT to the break-out board.

Operating the N5102A Module

This section shows you how to set the parameters for the N5102A module using the signal generator UI. Each procedure contains a figure that shows the softkey menu structure for the interface module function being performed. A quick reference setup checklist is also provided; see "Setup Checklist" on page 69.

Setting up the Signal Generator Baseband Data

The digital signal interface module receives data from a baseband source and outputs a digital IQ or digital IF signal relative to the selected logic type. Because an ESG/PSG provides the baseband data, the first procedure in operating the interface module is configuring the ESG/PSG using either one of the real-time or ARB modulation formats, or playing back your own file using the Dual ARB player. For information on configuring the ESG, refer to the *Agilent ESG Vector Signal Generator User's Guide*, and for configuring the PSG, refer to the *Agilent PSG Signal Generators User's Guide*.

1. Preset the signal generator.

2. Access the modulation format (TDMA, Custom, etc.) and set the desired parameters.

3. Turn-on the modulation format.

Accessing the N5102A Module User Interface

All parameters for the N5102A module are set with the UI on the ESG/PSG signal generator.

Press **Aux Fctn** > **N5102A Interface**.

This accesses the UI (first-level softkey menu shown in Figure 4-9) for configuring the digital signal interface module. Notice that there is a graphic, in the ESG/PSG display, showing a setup where the N5102A module is generating its own internal clock signal. This graphic changes to reflect the current clock source selection.

Figure 4-9   **First-Level Softkey Menu**
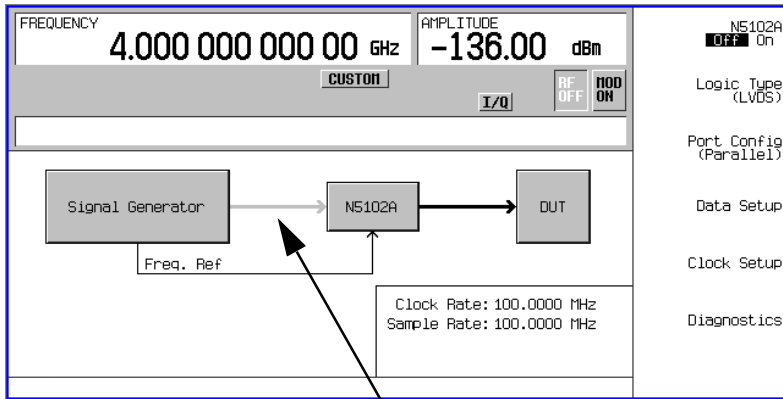
Line is grayed out until the N5102A module interface is turned on

Choosing the Logic Type and Port Configuration

Figure 4-10   **Logic and Port Configuration Softkey Menus**
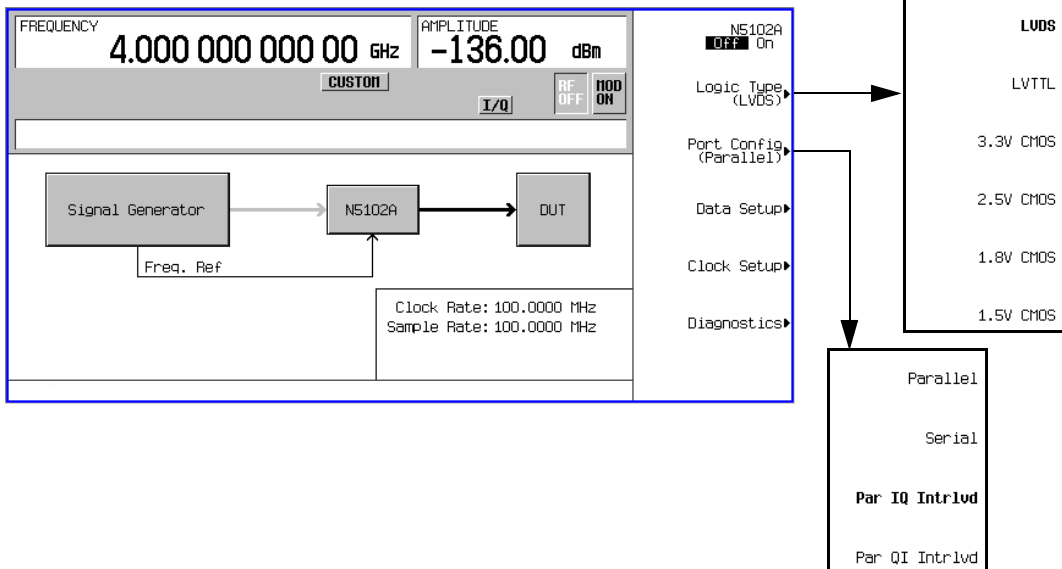
1. Refer to Figure 4-10. Press the **Logic Type** softkey.

    In this menu you can choose from a wide selection of logic types.

CAUTION	Changing the logic type can increase or decrease the signal voltage level going to the DUT. To avoid damaging the DUT and/or the N5102A module, ensure that both are capable of handling the voltage change.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

2. Select the logic type required for your DUT.

A caution message is displayed whenever you change logic types, and a softkey selection appears prompting you to confirm or cancel the logic type change.

3. Refer to Figure 4-10. Press the **Port Configuration** softkey.

In this menu you can select either a serial, parallel, or parallel interleaved data transmission.

Within the data and clock setup softkey menus, some softkeys function relative to the selected port configuration. So when you see softkeys that are grayed out, it generally means that they are not active for the current port configuration selection.

4. Select the port configuration for your DUT.

Selecting the Data Parameters

This procedure guides you through the data setup menu. Softkeys that have self-explanatory names are generally not mentioned. For example, the **Word Size** softkey. For more information on all of the softkeys, refer to "Softkey and SCPI Command Descriptions" on page 72.

1. Refer to Figure 4-11. Press the **Data Setup** softkey.

Figure 4-11   **Data Setup Menu Location**
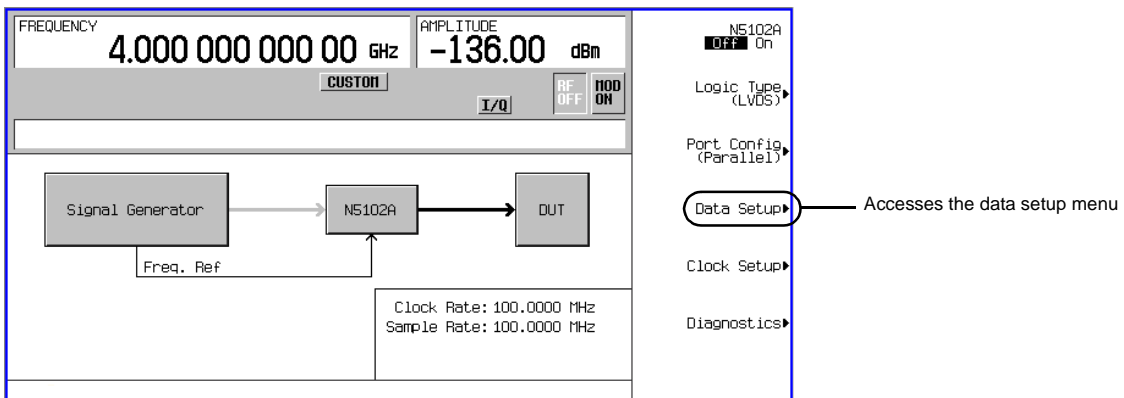
Within this softkey menu you can set the various parameters that govern the data received by the DUT. The status area of the display shows the number of data lines used for both I and Q along with the clock position relative to the data. When parallel or parallel interleaved is the port configuration, the number of data lines indicated is equivalent to the word (sample) size. When serial is the port configuration, the display will show that only one I and one Q data line is being used along with the frame marker that delineates the beginning of a sample. Figure 4-12 shows the data setup menu structure.

Figure 4-12   Data Setup Softkey Menu with Parallel Port Configuration
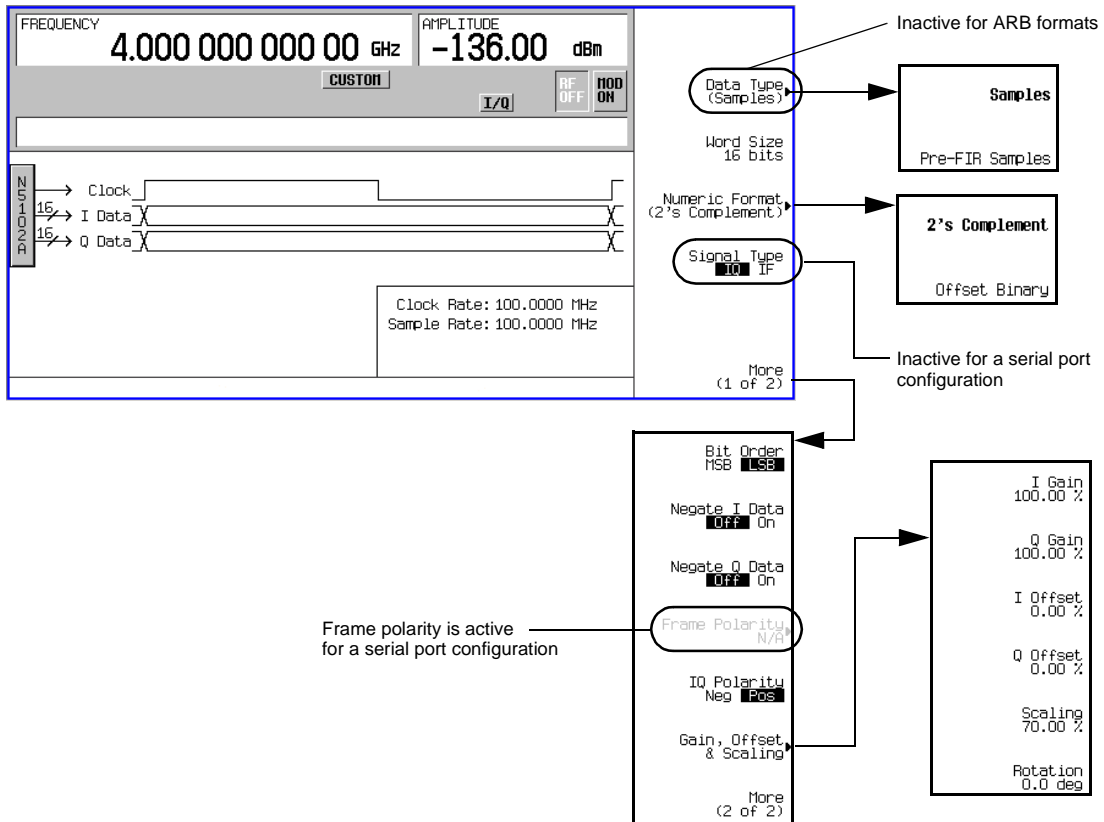
2. If you are using a real-time modulation format, press the **Data Type** softkey. (This softkey is inactive when an ARB modulation format is turned on.)

In this menu, you can select whether the real-time baseband data from the signal generator is either filtered (**Samples**) or unfiltered (**Pre-FIR Samples**). Your selection is dependent on your test needs and the DUT. The **Samples** selection provides FIR filtered baseband samples according to the communication standard (TDMA, W-CDMA, etc.) being used. This is the preset selection and the one most commonly

utilized. However if the DUT being tested already incorporates FIR filters, the **Pre-FIR Samples** selection should be used to avoid double filtering.

3. Select the data type that is appropriate for your test needs.

4. Press the **Numeric Format** softkey.

   From this menu, you can select how the binary values are represented. 2's complement allows both positive and negative data values. When components cannot process negative values, you can use the Offset Binary selection.

5. Select the numeric format required for your testing needs.

6. Press the **More (1 of 2)** softkey.

   From the second page of the softkey menu, you can select the bit order, the polarity of the transmitted data, and access another menu that provides scaling, gain, offset, and IQ rotation adjustments.

   Negation of the I and/or Q data is also a choice. Negation differs from changing the I and Q polarity: changing polarity is done at the bit level and merely changes a high to a low (1 to 0) and a low to a high (0 to 1) whereas negation is applied to a sample and it is the equivalent to multiplying the value of each sample by negative one.

   Negation changes the affected sample by expressing it in the two's complement form, multiplying it by negative one, and converting the sample back to the selected numeric format. This can be done for I samples, Q samples, or both. The choice to use negation is dependent on the DUT and how it needs to receive the data

7. Press the **Gain, Offset & Scaling** softkey.

   From this softkey menu you can:.

   - reduce word values for both I and Q using the **Scaling** softkey
   - increase or decrease the word values independently for I and Q using the **I Gain** and **Q Gain** softkeys
   - compensate for or add a DC offset using the **I Offset** and **Q Offset** softkeys
   - rotate the data on the IQ plane using the **Rotation** softkey

8. Make any required scaling, gain, offset, and/or rotation adjustments for properly testing your DUT.

9. Press **Return** > **Return** to return to the first-level softkey menu.

Configuring the Clock Signal

1. Refer to Figure 4-13. Press the Clock Setup softkey.

Figure 4-13   Clock Setup Menu Location
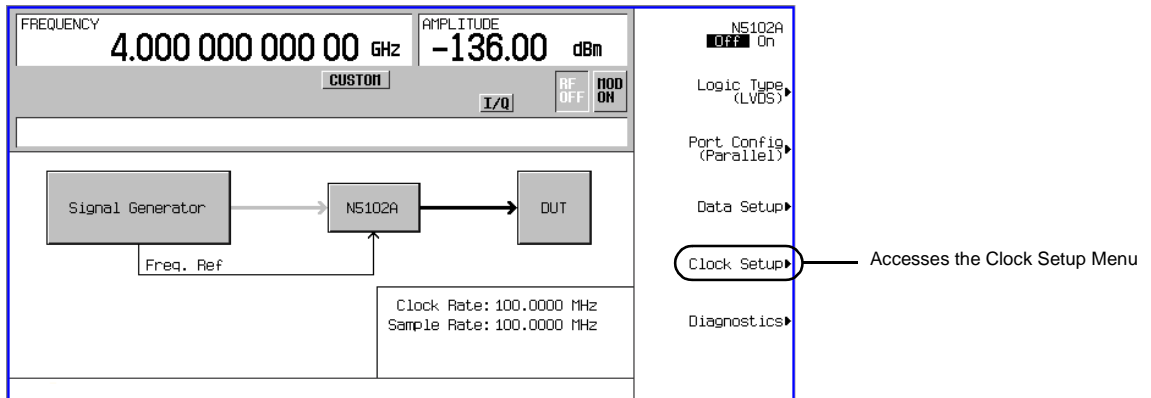
From this softkey menu, you set all of the clock parameters that synchronize the data between the N5102A module and the DUT. You can also change the clock signal phase so the clock occurs during the valid portion of the data. Figure 4-14 shows the clock setup menu.

Figure 4-14   Clock Setup Softkey Menu for a Parallel Port Configuration
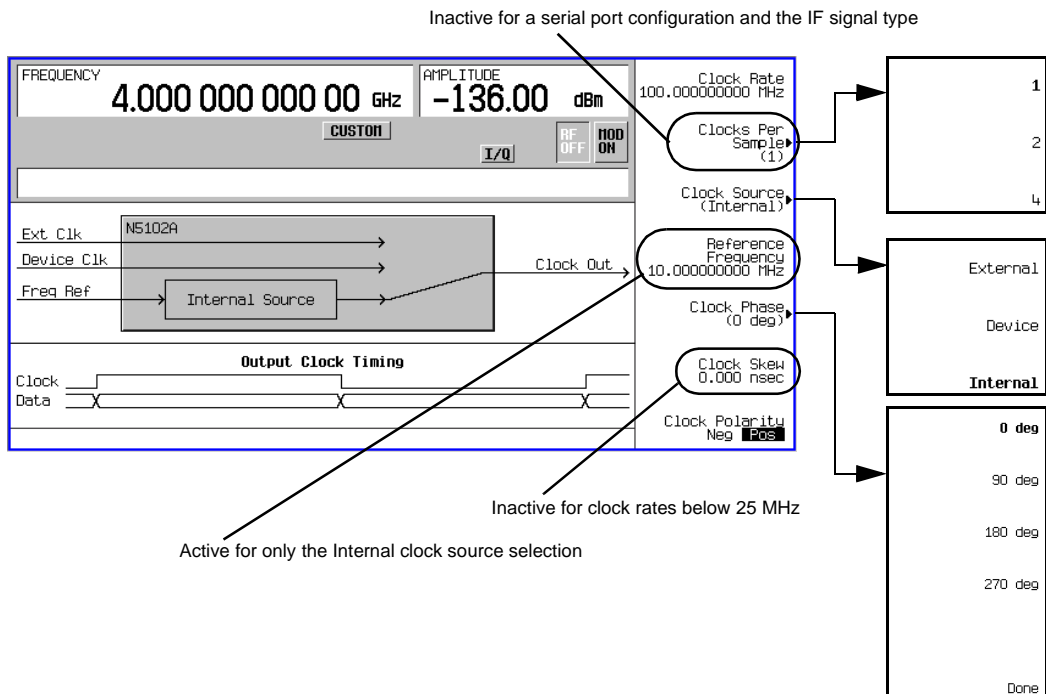
The top graphic on the display shows the current clock source that provides the output clock signal at the Clock Out and Device Interface connectors. The Clock Out line connection changes to reflect the clock source selection discussed later in this procedure. The bottom graphic shows the clock position relative to the data. The displayed clock signal will change to reflect the following:

- clocks per sample selection
- clock phase choice
- clock skew adjustment
- clock polarity selection

2. If parallel or parallel interleaved is the port configuration using an IQ signal type, press the **Clocks Per Sample** softkey.

   Notice that you can select multiple clocks per sample. Some DACs require the ability to clock multiple times for each sample, however having a clocks per sample value greater than one reduces your sample rate by a factor equal to the multiple clock selection. The sample rate is viewed on the first-level and Data Setup softkey menus.

3. Select the clocks per sample value to fit your test needs.

4. Press the **Clock Source** softkey.

   From this menu, select the clock signal source. With each selection, the clock routing display in the signal generator clock setup menu will change to reflect the current clock source. This will be indicated by a change in the Clock Out connection.

5. Select the clock source.

   If External or Device is Selected

   Press the **Clock Rate** softkey and enter the clock rate of the externally applied clock signal.

   For the **External** selection, the signal is supplied by an external clock source and applied to the Ext Clock In connector. For the **Device** selection, the clock signal is supplied via the Device Interface connector, generally by the DUT.

   If Internal is Selected

   Using a frequency reference, the N5102A module generates its own internal clock signal. The reference frequency is applied to the Freq Ref connector.

   a. Press the **Reference Frequency** softkey and enter the frequency of the externally applied frequency reference.

   b. Press the **Clock Rate** softkey and enter your clock rate.

   Table 4-5 provides a quick view of the settings and connections associated with each clock source selection.

Table 4-5   Clock Source Settings and Connectors

Clock Source	Softkeys		N5102A Module Connection		
	Reference Frequency	Clock Rate[1]	Freq Ref	Ext Clock In	Device Interface
External		●		●	
Device		●			●
Internal[2]	●	●	●		

1. For the Internal selection, this sets the internal clock rate. For the External and Device selections, this
   tells the interface module the rate of the applied clock signal.
2. There should be no clock signal applied to the Ext Clock In connector.

6. Press the **Clock Phase** softkey.

   From the menu that appears, you can adjust the phase of the clock relative to the data in 90 degree
   increments. The selections provide a coarse adjustment for positioning the clock on the valid portion of
   the data. Selecting 180 degrees is the same as selecting a negative clock polarity.

   The 90 and 270 degree selections are not available when the clock rate is set below 10 MHz or above
   200 MHz. If 90 or 270 degrees is selected when the clock rate is set below 10 MHz or above 200 MHz,
   the phase will change to 0 or 180 degrees, respectively.

7. Enter the required phase adjustment.

8. Press the **Return** softkey to return to the clock setup menu.

9. Press the **Clock Skew** softkey.

   This provides a fine adjustment for the clock relative to its current phase position. The skew is a phase
   adjustment using increments of time. You will realize greater skew adjustment capability at higher clock
   rates. For clock rates below 25 MHz, this softkey is inactive.

   The skew has discrete values with a range that is dependent on the clock rate. Refer to "Clock Timing for
   Phase and Skew Adjustments" on page 56 to determine the available skew settings for the current clock
   rate.

10. Enter the skew adjustment that best positions the clock with the valid portion of the data.

11. Press the **Clock Polarity Neg Pos** softkey to Neg.

    This shifts the clock signal 180 degrees, so that the data starts during the negative clock transition. This
    has the same affect as selecting the 180 degree phase adjustment.

12. Make the clock polarity selection that is required for the DUT.

13. Press the **Return** hardkey to return to the first-level softkey menu.

The clock source selection is also reflected in the first-level softkey menu graphic. For example, if the DUT is the new clock source, you will see that the frequency reference is now connected to the DUT and the DUT has an input clock line going to the N5102A module.

Generating Digital Data

Press the **N5102A Off On** softkey to On.

Digital data is now being transmitted from the N5102A module to the DUT. The green status light should be blinking. This indicates that the data lines are active. If the status light is solidly illuminated (not blinking), this indicates that all the data lines are inactive. The status light comes on and stays on (blinking or solid) after the first time the N5102A module is turned on (**N5102A Off On** to On). The status light will stay on until the module is disconnected from its power supply.

The interface module can only be turned on while a modulation format is active. If the modulation format is turned off while the module is on, the module will turn off and an error will be reported.

NOTE   If changes are made to the baseband data parameters, it is recommended that you first disable the digital output (**N5102A Off On** softkey to Off) to avoid exposing your DUT and the N5102A module to the signal variations that may occur during the parameter changes.

Setup Checklist

The setup checklist (Table 4-6) is a quick reference for configuring the digital signal interface module. The checklist shows each function for setting up the N5102A module along with a cross reference to the procedure that provides more detail.

Table 4-6   Setup Checklist

√	Function	Procedure
	Select logic type	"Choosing the Logic Type and Port Configuration" on page 61
	Select port configuration	
	Select filtered or unfiltered samples	"Selecting the Data Parameters" on page 62
	Enter word size	
	Select offset binary or 2's complement numeric format	
	Parallel & parallel interleaved mode—select IF or IQ output signal	
	Choose LSB or MSB data order	
	Negate and/or invert I and Q data	
	Serial mode—set frame marker polarity	
	Enter gain, scaling, offset, and IQ plane rotation values	
	Select clock source	"Configuring the Clock Signal" on page 64
	Enter clock rate	
	Parallel & parallel interleaved mode—select clocks per sample value	
	Internal clock source—enter reference frequency	
	Select clock polarity	
	Configure clock phase and skew	

5 Softkeys and SCPI Commands

This chapter describes the softkeys and SCPI commands for the N5102A Baseband Studio digital signal interface module. Softkeys and SCPI commands that perform the same function are documented together.

Softkey and SCPI Command Descriptions

0 deg

This softkey aligns the transition edge of the clock with the beginning of each sample for a parallel or parallel interleaved data transmission and with each bit for a serial data transmission. This is the factory preset phase selection.

Figure 5-1　　　　　　　**Clock Relative to the Data at 0 Degrees**
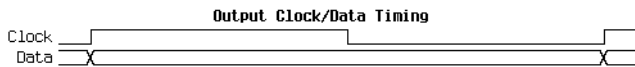
SCPI　　　　　　　:DIGital:CLOCk:PHASe 0
　　　　　　　　　:DIGital:CLOCk:PHASe?

1

For a parallel or parallel interleaved port configuration, this softkey selects one clock per sample. This is the factory preset selection. With either a serial port configuration or an IF signal type, this softkey is not accessible. For port configuration information, see "Port Config" on page 88; for signal type information, see "Signal Type IQ IF" on page 91.

SCPI　　　　　　DIGital:CLOCk:CPS 1
　　　　　　　　Digital:CLOCk:CPS?

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all three states (clocks per sample, port configuration, and signal type) to know the signal generator's current setup.

1.5V CMOS

This softkey sets the N5102A module output logic type to a 1.5 volt CMOS signal.

CAUTION Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI :DIGital:LOGic[:TYPE] CMOS15
:DIGital:LOGic[:TYPE]?

1.8V CMOS

This softkey sets the N5102A module output logic type to a 1.8 volt CMOS signal.

CAUTION Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI :DIGital:LOGic[:TYPE] CMOS18
:DIGital:LOGic[:TYPE]?

2

For a parallel or parallel interleaved port configuration, this softkey selects two clocks per sample. With either a serial port configuration, or an IF signal type, this softkey is not accessible. For port configuration information, see "Port Config" on page 88; for signal type information, see "Signal Type IQ IF" on page 91.

SCPI DIGital:CLOCk:CPS 2
DIGital:CLOCk:CPS?

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all three states (clocks per sample, port

configuration, and signal type) to know the signal generator's current setup.

2's Complement

This softkey sets the N5102A module output data format for a two's complement representation of the data values. This is the factory preset selection.

SCPI   :DIGital:DATA:NFORmat TCOMplement
              :DIGital:DATA:NFORmat?

2.5V CMOS

This softkey sets the N5102A module output logic type to a 2.5 volt CMOS signal.

CAUTION	Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI   :DIGital:LOGic[:TYPE] CMOS25
              :DIGital:LOGic[:TYPE]?

3.3V CMOS

This softkey sets the N5102A module output logic type to a 3.3 volt CMOS signal. This is the factory preset logic type.

CAUTION	Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI   :DIGital:LOGic[:TYPE] CMOS33
              :DIGital:LOGic[:TYPE]?

4

For a parallel or parallel interleaved port configuration, this softkey selects four clocks per sample. With either a serial port configuration, or an IF signal type, this softkey is not accessible. For port configuration information, see "Port Config" on page 88; for signal type information, see "Signal Type IQ IF" on page 91.

SCPI   DIGital:CLOCk:CPS 4
                DIGital:CLOCk:CPS?

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all three states (clocks per sample, port configuration, and signal type) to know the signal generator's current setup.

90 deg

This softkey provides a 90 degree phase adjustment for the clock signal. The phase adjustment moves the clock transition edge relative to the beginning of each sample for a parallel or parallel interleaved data transmission and to each bit during a serial data transmission.

This phase selection is unavailable (key is grayed out) when the clock rate is less than 10 MHz or greater than 200 MHz. If 90 degrees is the phase setting when the clock rate is changed to a value that is less than 10 MHz or greater than 200 MHz, the phase setting becomes zero degrees.

Figure 5-2   Clock Relative to the Data at 90 Degrees
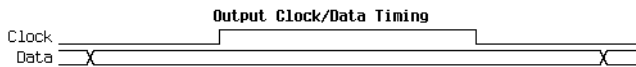
SCPI   :DIGital:CLOCk:PHASe 90
                :DIGital:CLOCk:PHASe?

When the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes to 180 degrees, and the maximum phase becomes 180 degrees. If this command is executed under these conditions, the phase becomes 180 degrees.

180 deg

This softkey provides a 180 degree phase adjustment for the clock signal. The phase adjustment is relative to the beginning of each sample for a parallel or parallel interleaved data transmission and to each bit during a serial data transmission. This functions the same as selecting the negative clock polarity using the **Clock Polarity Neg Pos** softkey.

Figure 5-3   **Clock Relative to the Data at 180 Degrees**
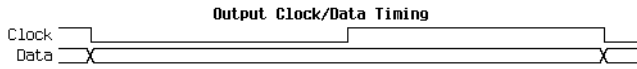
SCPI   :DIGital:CLOCk:PHASe 180
                :DIGital:CLOCk:PHASe?

270 deg

This softkey provides a 270 degree phase adjustment for the clock signal. The phase adjustment moves the clock transition edge relative to the beginning of each sample for a parallel or parallel interleaved data transmission and to each bit during a serial data transmission.

This phase selection is unavailable (key is grayed out) when the clock rate is less than 10 MHz or greater than 200 MHz. If 270 degrees is the phase setting when the clock rate is changed to a value that is less than 10 MHz or greater than 200 MHz, the phase becomes 180 degrees.

Figure 5-4   **Clock Relative to the Data at 270 Degrees**
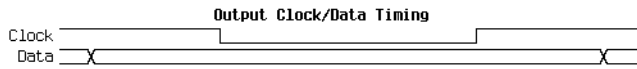
SCPI   :DIGital:CLOCk:PHASe 270
                :DIGital:CLOCk:PHASe?

When the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes to 180 degrees, and the maximum phase becomes 180 degrees. If this command is executed under these conditions, the phase setting becomes 180 degrees.

Bit Order MSB LSB

This softkey selects the bit ordering of the data that is passed from the N5102A module to the DUT.

MSB   This selection transmits the most significant bit (MSB) on data line zero for both I and Q for a parallel or parallel interleaved port configuration, and transmits the MSB as the first bit in a sample for a serial port configuration.

LSB   This selection transmits the least significant bit (LSB) on data line zero for both I and Q for a parallel or parallel interleaved port configuration, and transmits the LSB as the first bit in a sample for a serial port configuration.

For information on selecting the port configuration, see "Port Config" on page 88.

Preset	LSB
SCPI	`:DIGital:DATA:BORDer MSB|LSB`
	`:DIGital:DATA:BORDer?`

Clock Phase

This softkey accesses a menu that enables the phase adjustment (in 90 degree increments) of the clock edge relative to the start of each sample for a parallel or parallel interleaved data transmission, and to each data bit for a serial data transmission.

In addition to making coarse adjustments, the ESG/PSG also provides a fine-skew adjustment. See "Clock Skew" on page 79 for more information.

Preset	0 deg
SCPI	`:DIGital:CLOCk:PHASe 0|90|180|270`
	`:DIGital:CLOCk:PHASe?`

When the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes from 90 to 180 degrees, and the maximum phase becomes 180 degrees.

Clock Polarity Neg Pos

This softkey selects which clock edge (rising or falling) is aligned with the start of a sample for a parallel or parallel interleaved data transmission, and with the start of each bit for a serial data transmission. The Neg selection functions the same as selecting the 180 degree phase adjustment using the 180 deg softkey.

Preset	Pos
SCPI	`:DIGital:CLOCk:POLarity POSitive|NEGative`
	`:DIGital:CLOCk:POLarity?`

Clock Rate

This softkey enables you to adjust the clock rate (frequency) when the internal clock is used, or to enter the clock rate of an external clock source (connected at the Ext Clock In connector or supplied through the Device Interface connector). The value set with this softkey is also the rate for the output clock signal at the Clock Out connector and the Device Interface connector. See "Clock Source" on page 79 for information on selecting the clock source.

The clock rate range is dependent on the port configuration, logic type, signal type, and clocks per sample. Signal type and clocks per sample apply to parallel and parallel interleaved transmissions. The maximum frequency limits for the conditions are shown in the tables located in the Range field. The resolution for the clock rate is in millihertz. The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

Preset   100.000000000 MHz

Range

Parallel & Parallel Interleaved Port Configuration

Clocks Per Sample	Signal Type	LVTTL and CMOS Logic Type	LVDS Logic Type
1		1 kHz–100 MHz	1 kHz–100 MHz
2	IQ	2 kHz–150 MHz	2 kHz–200 MHz
4		4 kHz–150 MHz	4 kHz–300 MHz
1	IF	4 kHz–150 MHz	4 kHz–400 MHz

Serial Port Configuration

Word Size	LVTTL and CMOS Logic Type	LVDS Logic Type
4	4 kHz–150 MHz	4 kHz–300 MHz
5	5 kHz–150 MHz	5 kHz–300 MHz
6	6kHz–150 MHz	6 kHz–300 MHz
7	7 kHz–150 MHz	7 kHz–300 MHz
8	8 kHz–150 MHz	8 kHz–300 MHz
9	9 kHz–150 MHz	9 kHz–300 MHz
10	10 kHz–150 MHz	10 kHz–300 MHz
11	11 kHz–150 MHz	11 kHz–300 MHz
12	12 kHz–150 MHz	12 kHz–300 MHz
13	13 kHz–150 MHz	13 kHz–300 MHz
14	14 kHz–150 MHz	14 kHz–300 MHz
15	15 kHz–150 MHz	15 kHz–300 MHz
16	16 kHz–150 MHz	16 kHz–300 MHz

SCPI   :DIGital:CLOCk:RATE <val><unit>
                :DIGital:CLOCk:RATE?

Clock Setup

This softkey accesses a menu that enables you to select the clock and external frequency reference parameters that are used to synchronize the transmitted data from the N5102A module to the DUT.

Clock Skew

This softkey provides a fine-adjustment for aligning the clock to the valid portion of the data relative to the coarse adjustment associated with the **Clock Phase** softkey. Because this is a fine adjustment, it provides greater benefit at higher clock rates. When the clock rate is less than 25 MHz, this softkey is inactive (grayed out).

Skew is displayed in nanoseconds with a maximum range and a maximum number of discrete steps. Both the range and the number of steps are variable, and depend on the clock rate. The skew range contracts as the clock rate increases and expands as the clock rate decreases. The maximum skew range is reached at a clock rate of approximately 99 MHz and is maintained down to a clock rate of 25 MHz.

Preset	0.000 ns
Range	up to ±127 discrete steps, with a boundary of ±5 ns

$$\textit{Discrete Step Resolution: } \frac{1}{256 \times \text{Clock Rate}}$$

SCPI	:DIGital:CLOCk:SKEW <val><unit> :DIGital:CLOCk:SKEW?

Clock Source

This softkey accesses a menu where the clock source is selected. The selected clock source also provides the output clock signal at the Clock Out and Device Interface connectors.

CAUTION	It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

Preset	Internal
SCPI	:DIGital:CLOCk:SOURce EXTernal|DEVice|INTernal :DIGital:CLOCk:SOURce?

Clocks Per Sample

For a digital IQ signal, this softkey accesses a menu that enables you to select the number of clock cycles per sample, and is active for a parallel or parallel interleaved port configuration (see "Port Config" on page 88). For a serial port configuration, (or an IF signal) this softkey is grayed out (inactive). For a digital IF signal, this softkey is inactive (grayed out), and clocks per sample is fixed at one.

Some devices require multiple clocks per sample. The N5102A module provides multiple clocks per

sample choices (1x, 2x, or 4x). When you select a clocks per sample that is greater than one, the sample is held for that many clock cycles. This reduces the sample rate relative to the clock rate by a factor equal to the clocks per sample value. For example, if the clock rate is 100 MHz and you select four clocks per sample, the sample rate is 25 MHz.

For more information on clock rates, see "Clock Rate" on page 77. See also, "Clock and Sample Rates" on page 44.

Preset   1

SCPI   DIGital:CLOCk:CPS 1|2|4
                       DIGital:CLOCk:CPS?

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not *used* by the signal generator until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all three states (clocks per sample, port configuration, and signal type) to know the signal generator's current setup.

Data Setup

This softkey accesses a menu that enables you to set the parameters for data transmitted from the N5102A module to the DUT.

Data Type

This softkey accesses a menu that enables you to select either filtered baseband data or unfiltered baseband data from the ESG/PSG.

When an ARB modulation format is on, this softkey is inactive (grayed out) and the data type is samples.

Preset   Samples

SCPI   :DIGital:DATA:TYPE Samples|PFSamples
                       :DIGital:DATA:TYPE?

If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the signal generator until a real-time modulation format is turned on.

Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Device

This softkey selects the external clock signal that is provided through the Device Interface connector as the clock source for the N5102A module. You must also set the interface module clock rate to match that of the external clock signal (see "Clock Rate" on page 77). With this selection, the supplied clock is available as an output clock signal at the Clock Out and Device Interface connectors on the N5102A module.

| CAUTION | It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information. |

SCPI   :DIGital:CLOCk:SOURce DEVice
                  :DIGital:CLOCk:SOURce?

Device Intfc

This softkey selects a comprehensive loop back test that validates the delivery of digital data from the digital bus connector on the ESG/PSG to the Device Interface output connector on the N5102A module. Use this test to verify that the system is functioning properly after installation, or whenever the need arises. Running any loop back test turns off all active formats and the module. If this test fails, there are three other diagnostic tests that can help isolate the problem to the N5102A module, the digital bus cable, or the ESG/PSG. For information on these tests, see "SigGen Dig Bus" on page 90, "Dig Bus Cable" on page 81, and "N5102A Dig Bus" on page 85. To run the test, see "Run Loop Back Test" on page 89.

SCPI   :DIGital:DIAGnostic:LOOPback? DEVice

                  This command executes the diagnostic test, and returns the results of the test as pass or fail.

Diagnostics

This softkey accesses a menu where you can select and run N5102A module loop back tests.

Dig Bus Cable

This softkey selects a loop back test that verifies the output capability from the ESG/PSG Digital Bus connector to the end of the digital bus cable. This test requires the use of the loop back fixture board (supplied with the N5102A module). To run the test, see "Run Loop Back Test" on page 89.

SCPI   :DIGital:DIAGnostic:LOOPback? DCABLe

                  This command executes the diagnostic test and returns the results of the test as pass or fail.

External

This softkey selects the external clock signal provided through the Ext Clock in connector as the clock source for the N5102A module. You must also set the interface module clock rate to match that of the external clock signal (see "Clock Rate" on page 77). With this selection, the external clock is available as an output clock signal at the Clock Out and Device Interface connectors on the N5102A module.

CAUTION	It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

SCPI   :DIGital:CLOCk:SOURce EXTernal
                :DIGital:CLOCk:SOURce?

Frame Polarity Neg Pos

This softkey sets the polarity of the frame marker that delineates the beginning of each sample during a serial data transmission.

Neg   The frame line is low while data for the first sample is available.

Pos   The frame line is high while data for the first sample is available.

The frame marker is not effected by phase and skew adjustments.

For a parallel port configuration, this softkey is inactive (grayed out). For information on selecting serial data, see "Port Config" on page 88.

Preset   Pos

SCPI   :DIGital:DATA:POLarity:FRAMe NEGative|POSitive
                :DIGital:DATA:POLarity:FRAMe?

If this command is executed with a parallel or parallel interleaved port configuration, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to serial.

Because a query returns the currently set value, regardless of the port configuration, you must query both states (frame polarity and port configuration) to know the signal generator's current setup.

Gain, Offset & Scaling

This softkey accesses a menu that enables you to set the gain, DC offset, scaling, and IQ rotation for the N5102A module output data.

I Gain

This softkey sets the gain for the N5102A module output I data. This is a fine adjustment that is independent of the Q data and can be used to complement the setting obtained using the **Scaling** softkey.

Preset	100.0%
Range	87.50–112.5%
SCPI	:DIGital:DATA:IGain <val>
	:DIGital:DATA:IGain?

I Offset

This softkey sets the DC offset for the N5102A module output I data. The offset can be used to compensate for an existing impairment or to introduce an impairment to the I data.

Preset	0.00%
Range	-100 to 100% of full scale
SCPI	:DIGital:DATA:IOFFset <val>
	:DIGital:DATA:IOFFset?

Internal

This softkey selects the N5102A module internal clock as the clock source. This requires that the same external reference frequency be applied to both the Freq Ref connector and the ESG/PSG. You must also set the interface module reference frequency to match that of the applied signal (see "Reference Frequency" on page 89). This is the factory preset clock source selection. With this selection, the internal clock signal is available at the Clock Out and Device Interface connectors on the N5102A module.

CAUTION	It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

SCPI	:DIGital:CLOCk:SOURce INTernal
	:DIGital:CLOCk:SOURce?

IQ Polarity Neg Pos

This softkey sets the polarity of the I and Q output data lines for the N5102A module.

Neg	The output data on both the I and Q data lines are inverted. A digital one is represented by a low logic level at the output.

Pos   The polarity of the output data matches the input data. A digital one is represented by a high logic level at the output.

Preset   Pos

SCPI   :DIGital:DATA:POLarity:IQ POSitive|NEGative
        :DIGital:DATA:POLarity:IQ?

Logic Type

This softkey accesses a menu that enables you to select the logic type for the N5102A module output data.

CAUTION   Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

Preset   3.3V CMOS

SCPI   :DIGital:LOGic[:TYPE] LVDS|LVTTl|CMOS33|CMOS25|
        CMOS18|CMOS15
        :DIGital:LOGic[:TYPE]?

Loop Back Test Type

This softkey accesses a menu where you can select different loop back tests to verify the operation of the ESG/PSG digital output and the N5102A module.

To run the tests, see "Run Loop Back Test" on page 89.

Preset   Device Intfc

SCPI   :DIGital:DIAGnostic:LOOPback? DIGBus|CABLe|N5102A|DEVice

        This command executes the selected diagnostic test and returns the results of the test as pass or fail.

LVDS

This softkey sets the output logic type for the N5102A module to low voltage differential signaling (LVDS).

CAUTION   Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI   :DIGital:LOGic[:TYPE] LVDS
                    :DIGital:LOGic[:TYPE]?

LVTTL

This softkey sets the output logic type for the N5102A module to a low voltage TTL signal.

CAUTION	Changing the logic type changes the output voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

The output levels for the logics types are not maintained to the maximum clock rates. See "Logic Type Output Levels" on page 44 for more information.

SCPI   :DIGital:LOGic[:TYPE] LVTTl
                    :DIGital:LOGic[:TYPE]?

N5102A Dig Bus

This softkey selects a loop back test that verifies the connection and data transfer capability between the ESG/PSG and the N5102A module. The loop back for this test occurs at the input of the N5102A module and ensures that the Digital Bus input connector is functioning properly. For selecting the comprehensive test that includes verifying the operation of the N5102A module Device Interface output connector, see "Device Intfc" on page 81. To run the test, see "Run Loop Back Test" on page 89.

SCPI   :DIGital:DIAGnostic:LOOPback? N5102A

                    This command executes the diagnostic test and returns the results of the test as pass or fail.

N5102A Interface

This softkey accesses menus that enable you to control and set the N5102A module parameters.

N5102A Off On

This softkey enables or disables the N5102A module.

The interface module can only be turned on while a modulation format is active. If the modulation format is turned off while the module is on, the module will turn off and an error will be reported.

When the N5102A Interface is on, the ESG/PSG continuously polls the N5102A module to ensure it is connected. If the ESG/PSG determines that the N5102A module is not connected, it reports an error.

This also occurs if power is not supplied to the N5102A module via the included power supply. If the module is disconnected while on, the interface turns off and reports an error.

NOTE	If the softkey selection is On while setting the ESG/PSG parameters, the device under test can be subject to all output variations that are produced by intermediate setting changes.

Preset	Off
SCPI	`:DIGital[:STATe] 0|1|OFF|ON` `:DIGital[:STATe]?`

Negate I Data Off On

This softkey enables or disables negation of the value of each sample for the I output. This is equivalent to multiplying the value of each sample by negative one. Negation changes the affected sample by expressing it in two's complement form, multiplying by negative one, and converting back to the selected numeric format. This can be done for I samples, Q samples (see Negate Q Data Off On), or both. The choice to use negation is dependent on the DUT and how it needs to receive the data.

On	The I data is negated.
Off	No negation is performed.
Preset	Off
SCPI	`:DIGital:DATA:INEGate 0|1|OFF|ON` `:DIGital:DATA:INEGate?`

Negate Q Data Off On

This softkey enables or disables negation of the value of each sample for the Q output. This is equivalent to multiplying the value of each sample by negative one. Negation changes the affected sample by expressing it in two's complement form, multiplying by negative one, and converting back to the desired numeric format. This can be done for I samples (see Negate I Data Off On), Q samples, or both. The choice to use negation depends on the DUT and how it needs to receive the data.

On	The Q data is negated.
Off	No negation is performed.
Preset	Off
SCPI	`:DIGital:DATA:QNEGate 0|1|OFF|ON` `:DIGital:DATA:QNEGate?`

Numeric Format

This softkey accesses a menu that enables you to select the binary format (representation) for the data values that are transmitted from the N5102A module to the DUT. There are two binary format choices, 2's complement and offset binary.

Preset   2's Complement

SCPI   :DIGital:DATA:NFORmat TCOMplement|OBINary
                            :DIGital:DATA:NFORmat?

Offset Binary

This softkey sets the N5102A module output data format to an offset binary representation of the data values. The choice of data format is dependent on the DUT and how it needs to receive the data.

SCPI   :DIGital:DATA:NFORmat OBINary
                            :DIGital:DATA:NFORmat?

Par IQ Intrlvd

This softkey enables parallel interleaving of the output data samples transmitted from the N5102A module to the DUT, where the I sample is transmitted before the Q sample.

For more information on parallel interleaved data transmissions, see "Clock Timing for Parallel Interleaved Data" on page 54.

SCPI   :DIGital:PCONFig PINTIQ
                            :DIGital:PCONFig?

Par QI Intrlvd

This softkey enables parallel interleaving of the output data samples transmitted from the N5102A module to the DUT, where the Q sample is transmitted before the I sample.

For more information on parallel interleaved data transmissions, see "Clock Timing for Parallel Interleaved Data" on page 54.

SCPI   :DIGital:PCONFig PINTQI
                            :DIGital:PCONFig?

Parallel

This softkey enables parallel data transmission from the N5102A module to the DUT. This is the factory preset port configuration.

SCPI   :DIGital:PCONFig PARallel
                            :DIGital:PCONFig?

Pre-FIR Samples

This softkey selects unfiltered data for the input of the N5102A module. When an ARB modulation format is on, this softkey is not accessible.

SCPI   :DIGital:DATA:TYPE PFSamples
                         :DIGital:DATA:TYPE?

If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the signal generator until a real-time modulation format is turned on.

Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Port Config

This softkey accesses a menu that enables you to select a parallel, serial, parallel interleaved IQ, or parallel interleaved QI data transmission between the N5102A module and the DUT.

Preset   Parallel

SCPI   :DIGital:PCONFig PARallel|SERial|PINTIQ|PINTQI
                         :DIGital:PCONFig?

Q Gain

This softkey sets the gain for the N5102A module output Q data. This is a fine adjustment, independent of the I data, that can be used to complement the setting obtained using the **Scaling** softkey.

Preset   100.0%

Range   87.50–112.5%

SCPI   :DIGital:DATA:QGain <val>
                         :DIGital:DATA:QGain?

Q Offset

This softkey sets the DC offset for the N5102A module output Q data. The offset can be used to compensate for an existing impairment or to introduce an impairment to the Q data.

Preset   0.00%

Range   −100 to 100% of full scale

SCPI   :DIGital:DATA:QOFFset <val>
                         :DIGital:DATA:QOFFset?

Reference Frequency

For the Internal source selection, this softkey specifies the frequency of the external reference supplied to the Freq Ref connector. The value set with this softkey enables the internal source of the N5102A module to lock onto the externally supplied reference.

CAUTION	The module can lock onto a signal that is within 6 MHz of the selected reference frequency. If you specify a frequency that is different from what is being supplied, you won't get the right output, and might not get an error.

This softkey is inactive (grayed out) for the External and Device clock source selections.

Preset   10.0000000 MHz

Range   1–100 MHz

SCPI   `:DIGital:CLOCk:REFerence:FREQuency <val><unit>`
                      `:DIGital:CLOCk:REFerence:FREQuency?`

If this command is executed when the clock source is not set to internal, the parameter value is changed, but it is not used by the signal generator until the clock source is changed to internal.

Because a query returns the currently set value, regardless of the clock source, you must query both states (reference frequency and clock source) to know the signal generator's current setup.

Rotation

Use this softkey to rotate the IQ constellation for the N5102A module output data.

Preset   0.0 deg

Range   0–360 degrees

SCPI   `:DIGital:DATA:ROTation <val>`
                      `:DIGital:DATA:ROTation?`

Run Loop Back Test

This softkeys starts the selected diagnostic loop back test and returns the results of the test as a pass or fail.

SCPI   `:DIGital:DIAGnostic:LOOPback? DIGBus|CABLe|N5102A|DEVice`

This command executes the selected loop back test and returns the results of the test as pass or fail.

Samples

This softkey selects ESG/PSG filtered samples as the baseband data for the input. This is the factory preset data type. When an ARB modulation format is on, this softkey is not accessible.

SCPI   `:DIGital:DATA:TYPE Samples`
                        `:DIGital:DATA:TYPE?`

                        If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the signal generator until a real-time modulation format is turned on.

                        Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Scaling

This softkey scales the output I and Q data for the N5102A module. This feature is primarily used to remove overrange errors.

Preset   70.00%

Range   -100 to 100%

SCPI   `:DIGital:DATA:SCALing <val>`
                        `:DIGital:DATA:SCALing?`

Serial

This softkeys enables serial data transmission from the N5102A module to the DUT.

SCPI   `:DIGital:PCONFig SERial`
                        `:DIGital:PCONFig?`

SigGen Dig Bus

This softkey selects a loop back test that verifies the output capability of the ESG/PSG Digital Bus connector. This test requires the use of the loop back fixture board (supplied with the N5102A module). This is the factory preset loop back test selection. To run the test, see "Run Loop Back Test" on page 89.

SCPI   `:DIGital:DIAGnostic:LOOPback? DIGBus`

                        This command executes the diagnostic test and returns the results of the test as pass or fail.

Signal Type IQ IF

This softkey is applicable only for parallel and parallel interleaved data transmissions. The signal type softkey enables you to select the digital signal type for the output of the N5102A module. For a serial port configuration, this softkey is inactive (grayed out) and IQ shows as the signal type.

IQ	The output of the N5102A module is digital IQ data, which is applicable to both parallel/parallel interleaved and serial port configurations.
IF	The digital I and Q samples are combined, and modulated on an intermediate frequency (IF) carrier. The frequency of the IF (the center frequency of the modulated IF signal), is set to one-fourth of the sample rate (for example, for a 400 MHz clock rate, the IF is 100 MHz). This is available for only parallel and parallel interleaved data transmissions.
Preset	IQ
SCPI	`:DIGital:DATA:STYPe IQ│IF` `:DIGital:DATA:STYPe?`

If this command is executed with a serial port configuration, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to parallel or parallel interleaved.

Because a query returns the currently set value, regardless of the port configuration, you must query both states (signal type and port configuration) to know the signal generator's current setup.

Word Size

This softkey sets the number of bits in each sample transmitted from the N5102A module to the DUT. A word is defined as an integer number of bits from 4 to 16. For parallel and parallel interleaved data, Word is synonymous with sample. Any unused data lines are driven low.

Preset	16
Range	4–16
SCPI	`:DIGital:DATA:SIZE <val>` `:DIGital:DATA:SIZE?`

6 Troubleshooting

This chapter provides the following information to assist you in troubleshooting the N5102A Baseband Studio digital signal interface module:

- "If You Encounter a Problem" on page 94
- "Replaceable Parts" on page 100
- "Returning an Instrument to Agilent Technologies" on page 101

If You Encounter a Problem

CAUTION	Immediately unplug the N5102A module from the AC power line if the unit shows any of the following symptoms:

- Smoke, arcing, or unusual noise from inside the unit.
- A circuit breaker or fuse on the main AC power line opens.

These potentially serious faults must be corrected before proceeding.

If the signal generator displays an error, read the error message text by pressing **Utility** > **Error Info**. Resolve any problems specific to the signal generator (refer to the signal generator's documentation).

If the N5102A module is not operating properly (for example, it fails "Operation Verification" on page 11), refer to the following table to begin troubleshooting.

If the...	Do this...
Power LED is off	Go to "Checking Power Problems" on page 95
Power LED is on	Go to "Running Diagnostic Tests" on page 96
ESG/PSG has a persistent N5102A module error. A module error persists even after you fix the problem described in the error message and clear the error queue: **Utility** > **Error Info** > **Clear Error Queue(s)**	Reset the module (turn it off and then back on). If the error still persists, there is something wrong with the hardware. Contact Agilent (see page 101).

Checking Power Problems

When you connect the power supply to the module, the green Power LED should light.

If the Power LED does not light:

1. Check the power cord; ensure that it is:

   • in good condition

   • properly plugged in to a live outlet (line power connection is described on page 6)

   • properly connected to the power supply (power supply connection is described on page 10) and the DC power supply plug is fully inserted into the N5102A module DC power receptacle

   If this does not solve the problem, go to step 2 to check the power supply.

2. Using a DVM, check the power supply output.

   +4.7 to 5.3V
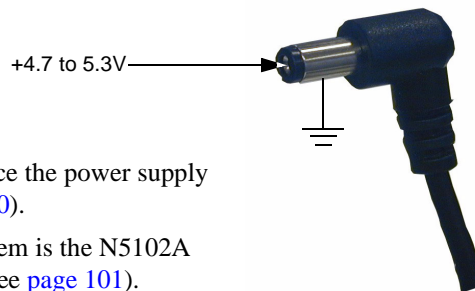
   If the output voltage is not correct, replace the power supply (refer to "Replaceable Parts" on page 100).

   If the output voltage is correct, the problem is the N5102A module. Return the module to Agilent (see page 101).

Running Diagnostic Tests

Diagnostic tests, referred to as loop back tests, are provided to assist in isolating a problem. Perform the tests in the order listed in the following table.

Test	Purpose	Loop Back Test Board Used
Device Interface *begin with this test, on* page 97	Checks the operation of the entire system, from the digital output of the signal generator to the N5102A module's Device Interface connector.	Loop Back Test Single Ended IO Dual 40 Pin board (shown on page 97; described in detail on page 29)
N5102A Digital Bus	Checks the input of the N5102A module.	None
Digital Bus Cable	Checks the communication path from the signal generator's Digital Bus connector to the end of the digital bus cable.	Digital bus loop back fixture (shown on page 98)
Signal Generator Digital Bus	Checks the signal generator digital output.	Digital bus loop back fixture (shown on page 99)

These tests (described in the following figure) are in the N5102A **Diagnostics** menu.
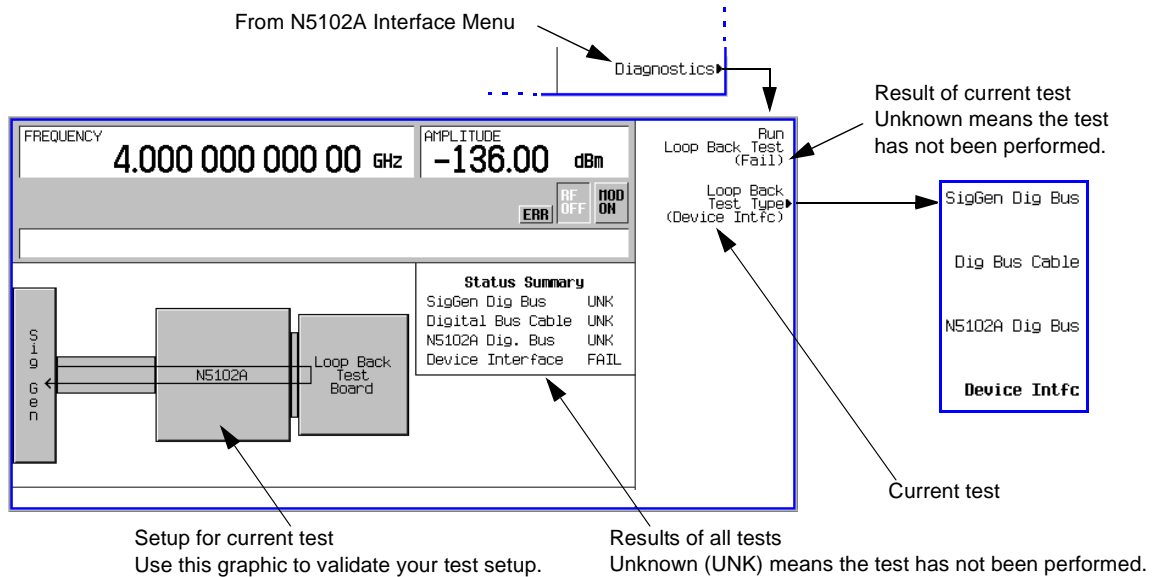
Device Interface (System) Test

This is a comprehensive test that checks the paths from the signal generator Digital Bus connector to the Device Interface connector on the N5102A module. This is the same test used in the section, "Operation Verification" on page 11, which describes the test in more detail.

1. Connect the N5102A module to the signal generator according to the steps in "Connecting the N5102A Module to the ESG/PSG" on page 8.

Connect to N5102A module

2. Connect the Loop Back Test Single Ended IO Dual 40 Pin board, shown at right, to the Device Interface connector on the rear of the N5102A module.

   Ensure that there are no connections to the two 40-pin connectors.

40-pin Connectors
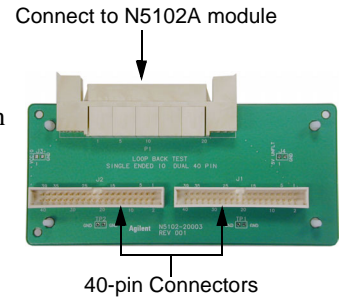
3. Select and run the Device Interface test:

   a. On the signal generator, press
      Aux Fctn > **N5102A Interface** > **Diagnostics** > **Loop Back Test Type** > **Device Intfc**.

      Note that the test selection in parentheses below the **Loop Back Test Type** softkey updates to reflect the current test.

   b. Press **Run Loop Back Test**.

      Because all signal generator modulation formats and the N5102A module interface must be off before a loop back test can run, if they are active when you press the **Run Loop Back Test** softkey, they turn off automatically.

- If this test passes and the N5102A module still has a problem, send the module to Agilent for service (see page 101).

- If this test fails, examine all connectors (they should be clean and undamaged) and connections (they must be secure). If the test still fails, perform the N5102A Digital Bus test to help isolate the problem.

N5102A Digital Bus Test

This test checks the communication path from the Digital Bus connector on the signal generator to the input of the N5102A module. It does not require the use of a loop back test board.

1. If not already done, disconnect the Loop Back Test Single Ended IO Dual 40 Pin board from the N5102A module.

   Leave all other connections.

2. Select and run the N5102A Digital Bus test:

   On the signal generator, press **Loop Back Test Type** > **N5102A Dig Bus** > **Run Loop Back Test**.

- If this test passes, the problem is with the N5102A module; send the module to Agilent for service (see page 101).

- If this test fails, perform the Digital Bus Cable test to further isolate the problem.

Digital Bus Cable Test

This test checks the communication path from the Digital Bus connector on the signal generator to the end of the digital bus cable. It requires the use of the digital bus loop back fixture.

1. Disconnect the digital bus cable from the N5102A module.

Release latches

Remember to press
the release latches when
connecting or disconnecting
the cable.
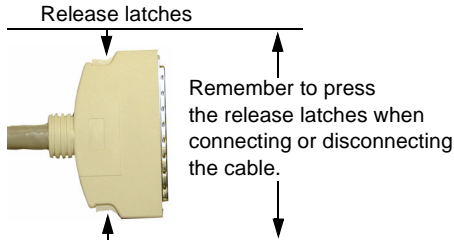
2. Check the connectors on the digital bus loop back fixture, shown at right, to ensure that they are clean and undamaged, then connect it securely to the digital bus cable in place of the module.

3. Select and run the Digital Bus Cable test:

   On the signal generator, press **Loop Back Test Type** > **Dig Bus Cable** > **Run Loop Back Test**.

Connect to the digital bus cable

- If this test passes, the problem is with the N5102A module; send the module to Agilent for service (see page 101).

- If this test fails, perform the Signal Generator Digital Bus test to further isolate the problem.

Signal Generator Digital Bus Test

This test checks the digital output capability of the signal generator and requires the use of the loop back fixture, shown at right.

Connect to the signal generator

1. Disconnect the digital bus loop back fixture from the digital bus cable.

2. Disconnect the digital bus cable from the signal generator, and connect the digital bus loop back fixture securely in its place.

3. Select and run the Signal Generator Digital Bus test

   On the signal generator, press **Loop Back Test Type** > **SigGen Dig Bus** > **Run Loop Back Test**.

- If this test passes, the problem is with the digital bus cable; replace the cable (see "Replaceable Parts" on page 100).

- If this test fails, the problem is with the signal generator; send the signal generator to Agilent for service (see page 101).
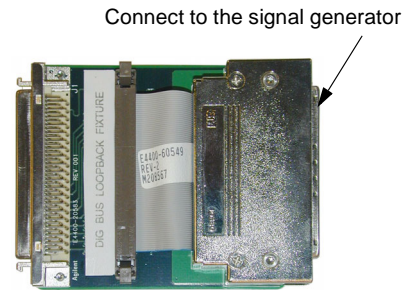
Replaceable Parts

Contact Agilent (see Table 6-1) for price and availability of the following parts.

Description	Part Number	Description	Part Number
Digital Bus Cable	N5101-60003	Power Cord	
Digital Bus Loop Back Fixture	E4400-63583	United Kingdom	N5102A-900
Loop Back Test Single Ended IO Dual 40 Pin Board	N5102-63003	Australia and New Zealand	N5102A-901
Single Ended I/O Dual 20 Pin Board	N5102-63004	Continental Europe	N5102A-902
Differential I/O 38 Pin Board	N5102-63005	United States and Canada, 120V	N5102A-903
Differential I/O Dual 100 Pin Board	N5102-63006	Switzerland	N5102A-906
Single Ended I/O 68 Pin Board	N5102-63007	Denmark	N5102A-912
N5102A User's Guide	N5102-90001	South Africa and India	N5102A-917
Documentation CD	N5102-90002	Japan	N5102A-918
Power Supply, AC-DC 5V 4A	0950-4540	Israel	N5102A-919
		Argentina	N5102A-920
		Chile	N5102A-921
		China	N5102A-922
		Brazil and Thailand	N5102A-927

Returning an Instrument to Agilent Technologies

1. Be prepared to give the service representative as much information as possible regarding the instrument's problem.
2. Either use the URL listed in Table 6-1 to locate your key contact, or call the phone number listed below that is appropriate to the instrument's location. After providing information about the instrument and the problems you are experiencing, you will receive instructions on where to ship the instrument for repair.
3. If they are available, use the original factory packaging materials. If not, use similar packaging to properly protect the instrument.

Table 6-1   **Contacting Agilent**

Online assistance: `www.agilent.com/find/assist`			
United States (tel) 1 800 452 4844	**Latin America** (tel) (305) 269 7500 (fax) (305) 269 7599	**Canada** (tel) 1 877 894 4414 (fax) (905) 282-6495	**Europe** (tel) (+31) 20 547 2323 (fax) (+31) 20 547 2390
New Zealand (tel) 0 800 738 378 (fax) (+64) 4 495 8950	**Japan** (tel) (+81) 426 56 7832 (fax) (+81) 426 56 7840	**Australia** (tel) 1 800 629 485 (fax) (+61) 3 9210 5947	
Asia Call Center Numbers			
Country	**Phone Number**		**Fax Number**
Singapore	1-800-375-8100		(65) 836-0252
Malaysia	1-800-828-848		1-800-801664
Philippines	(632) 8426802 1-800-16510170 (PLDT Subscriber Only)		(632) 8426809 1-800-16510288 (PLDT Subscriber Only)
Thailand	(088) 226-008 (outside Bangkok) (662) 661-3999 (within Bangkok)		(66) 1-661-3714
Hong Kong	800-930-871		(852) 2506 9233
Taiwan	0800-047-866		(886) 2 25456723
People's Republic of China	800-810-0189 (preferred) 10800-650-0021		10800-650-0121
India	1-600-11-2929		000-800-650-1101

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